

PAGE	CONTENTS
1	INDEX
2	BLOCK DIAGRAM
3	POWER DELIVERY
4	CHANGE LIST
5	CPU PCIEX16/DMI
6	CPU DDR CHANNEL A
7	CPU DDR CHANNEL B
8	CPU MISC
9	CPU POWER
10	CPU GND
11	DDR3 DIMMA1
12	DDR3 DIMMB1
13	PCH DMI/PCIE/USB
14	PCH CLINK/SATA/CPU HOST
15	PCH HDA/SPI/MISC
16	PCH LPC/DP/USB3/UART
17	PCH CLOCK BUFFER
18	PCH POWER
19	PCH GND
20	PCIEX16/X1*2 SLOT
21	RTD2168 EDP to VGA
22	DVI CONNECTOR
23	SIO IT8613E
24	SATA CONN
25	REAR USB
26	FRONT USB
27	LAN RTL8111H/8107E
28	AUDIO CODEC ALC887
29	AUDIO CONNECTOR
30	ACPI POWER
31	MEMORY DC-DC
32	V_1P0_PCH
33	RESUME RESET LOGIC
34	SUPERIO PS2/COM
35	FAN
36	24PIN CONN & FP
37	SPI ROM/RTC CRYSTAL/BAT
38	VCCIO/VCCSA DC-DC
39	RT3606 DC-DC CONVERTE
40	RT3606_VCORE_PHASE
41	RT3606_VGT_PHASE
42	BOM

# IH11M-MHS H110MD PRO D4 VER 6.0

CPU:  
Intel Skylake S 42 in LGA1151 Package 95W

System Chipset:  
SPT-H PCH

Main Memory:  
Dual Channel/DDR-4\*2(Max 16GB)1867/2133

Onboard Device:

Super I/O:IT8613E  
LAN:Realtek 8111H  
HD Codec:ALC887


Power solution:  
CPU Voltage Regulators:3phase by RT3606 high 1 Low 1 OV by RT3606  
DDR Voltage Regulators:1Phase by UP1514 high 1 Low 1 OV by IT8613E

Expansion Slots:  
PCI EXPRESS 16X SLOT \*1  
PCI EXPRESS 1X SLOT \*2

REAR IO:  
PS/2 PORT  
DVI Port  
VGA Port  
USB3.0 PORT \*2  
Gb RJ-45 +2 layer USB3.0 Ports  
Audio Jackets (3 PORT)

Front I/O:  
SATA3 \*6  
USB 2.0 Header \* 2 Serial header  
USB 3.0 Header \* 1 Front Audio Header  
CPU FAN \*1  
System FAN \*1

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Title INDEX		
Size B	Document Number IH11M-MHS	Rev 6.0
Date: Friday, January 08, 2016	Sheet 1	of 42

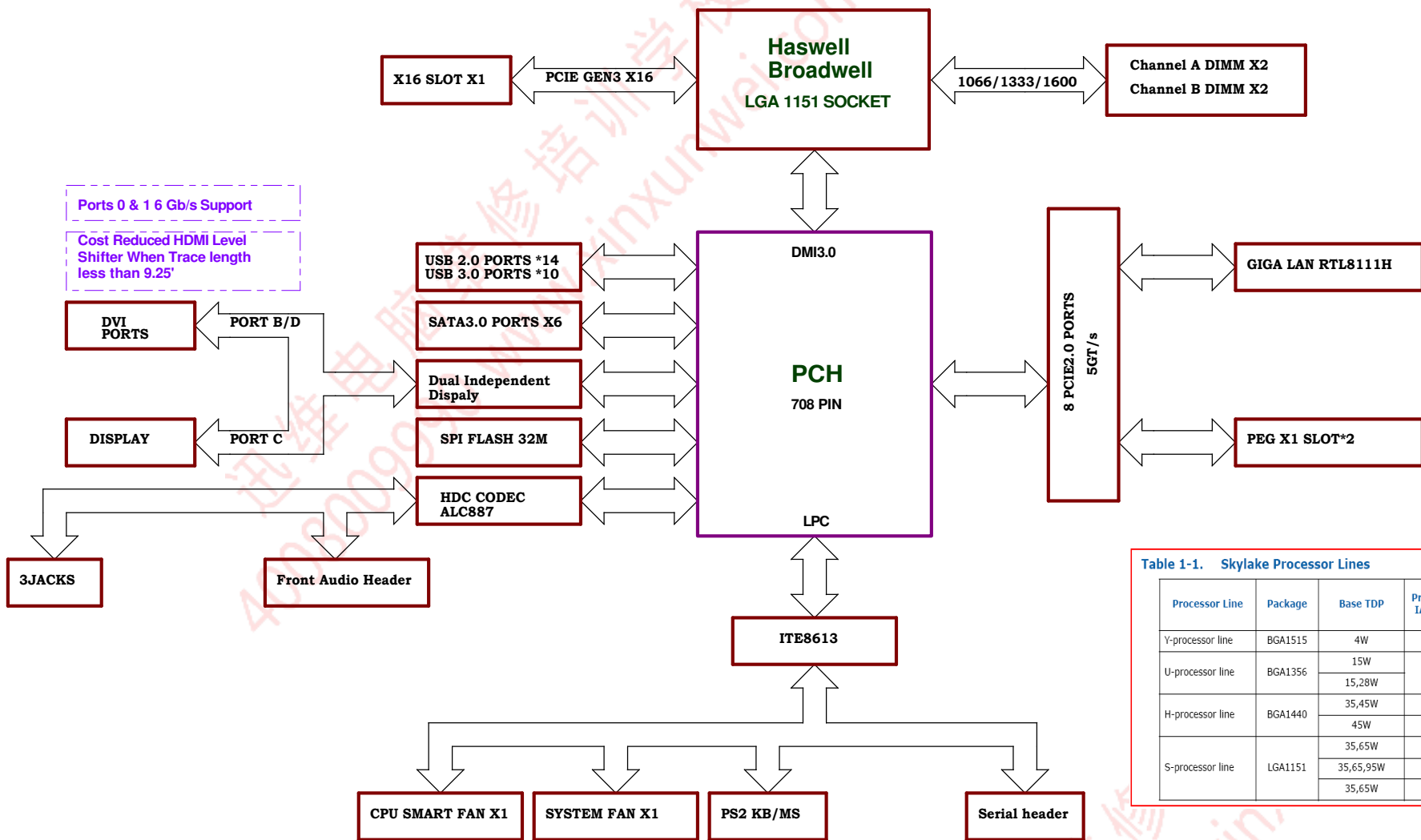


Table 1-1. Skylake Processor Lines						
Processor Line	Package	Base TDP	Processor IA Cores	Maximum Graphics Configuration	On Package Cache	Platform Type
Y-processor line	BGA1515	4W	2	GT2	N/A	1-Chip
U-processor line	BGA1356	15W	2	GT2	64 MB	1-Chip
		15,28W		GT3		
H-processor line	BGA1440	35,45W	4	GT2	N/A	2-Chip
		45W	4	GT4	128 MB	
S-processor line	LGA1151	35,65W	2	GT2	N/A	2-Chip
		35,65,95W	4	GT2		
		35,65W	4	GT4	64 MB	

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Title: **BLOCK DIAGRAM**

Size B	Document Number	Rev 6.0
Date: Friday, January 08, 2016		Sheet 2 of 42

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4008009990 www.xinxunwei.com

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Title		POWER DELIVERY	
Size B	Document Number IH11M-MHS		Rev 6.0
Date:	Friday, January 08, 2016	Sheet	3 of 42

1.VER0.60:COLAY S3 FUNCTION(PAGE15/23/25/26/28/30/31/32/33)

2.VER0.60:COLAY REMOVE VGT\_PH2(PAGE39)

3.VER0.60:DDR3 CHANGE DDR4(PAGE6/7/11/12)

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CPU PCIEX16/DMI/FDI

Title  
Size  
B

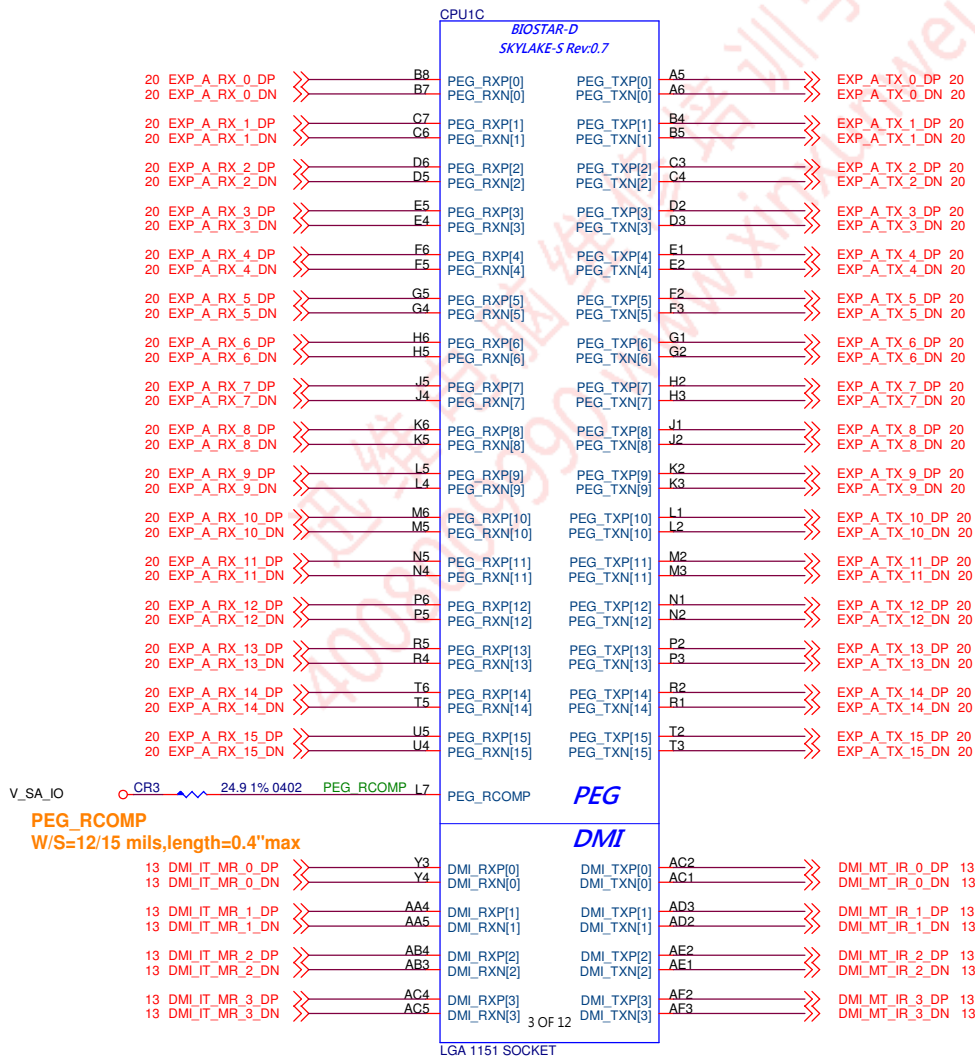
Document Number

IH11M-MHS

Rev  
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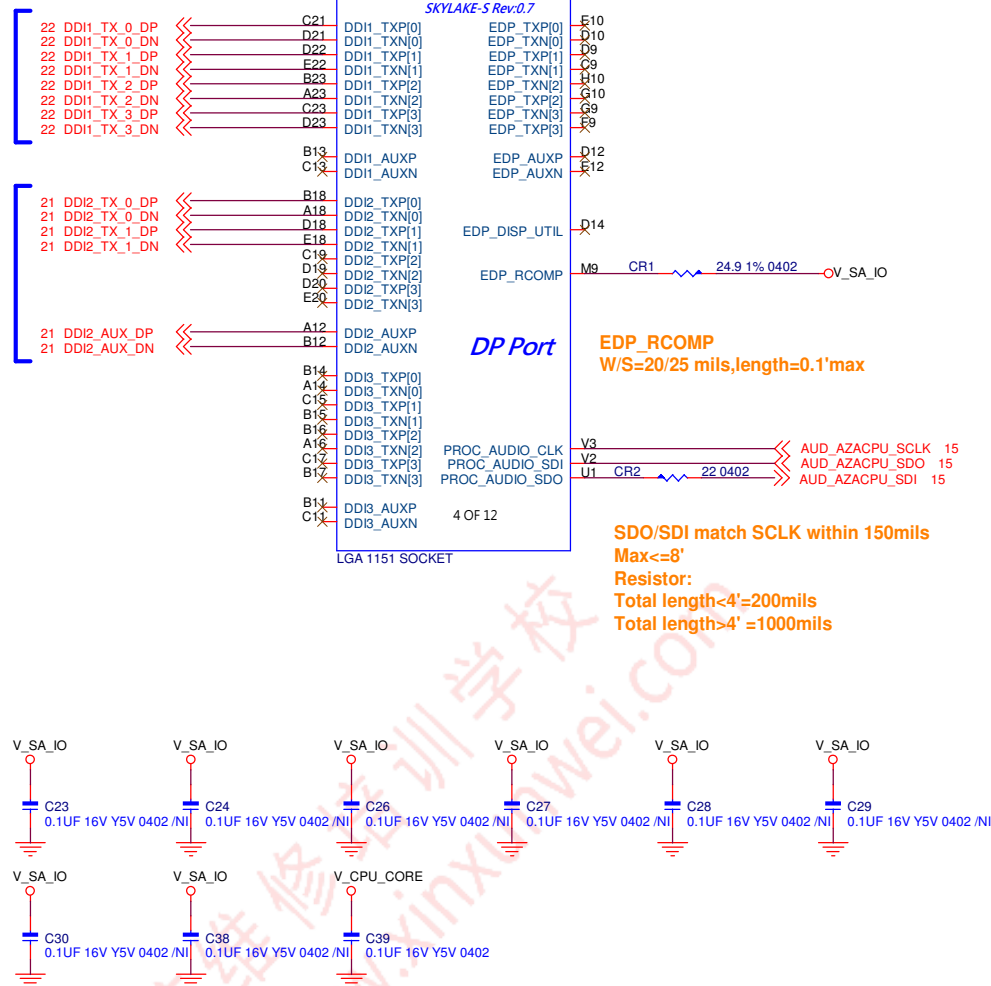
Date: Friday, January 08, 2016

Sheet 4 of 42



DVI PORT

EDP to VGA



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**CPU PCIEX16/DMI/FDI**

Size B Document Number  
**IH11M-MHS**

Date: Friday, January 08, 2016 Sheet 5 of 42

Rev 6.0





12 M\_DATA\_B[0..63] <<< M\_DATA\_B[0..63]

M_DATA_B0	AD34	DDR1_DQ[0]/DDR0_DQ[16]
M_DATA_B1	AD35	DDR1_DQ[1]/DDR0_DQ[17]
M_DATA_B2	AG35	DDR1_DQ[2]/DDR0_DQ[18]
M_DATA_B3	AH35	DDR1_DQ[3]/DDR0_DQ[19]
M_DATA_B4	AE35	DDR1_DQ[4]/DDR0_DQ[20]
M_DATA_B5	AE34	DDR1_DQ[5]/DDR0_DQ[21]
M_DATA_B6	AG34	DDR1_DQ[6]/DDR0_DQ[22]
M_DATA_B7	AH34	DDR1_DQ[7]/DDR0_DQ[23]
M_DATA_B8	AK35	DDR1_DQ[8]/DDR0_DQ[24]
M_DATA_B9	AL35	DDR1_DQ[9]/DDR0_DQ[25]
M_DATA_B10	AK32	DDR1_DQ[10]/DDR0_DQ[26]
M_DATA_B11	AL32	DDR1_DQ[11]/DDR0_DQ[27]
M_DATA_B12	AK34	DDR1_DQ[12]/DDR0_DQ[28]
M_DATA_B13	AL34	DDR1_DQ[13]/DDR0_DQ[29]
M_DATA_B14	AK31	DDR1_DQ[14]/DDR0_DQ[30]
M_DATA_B15	AL31	DDR1_DQ[15]/DDR0_DQ[31]
M_DATA_B16	AP35	DDR1_DQ[16]/DDR0_DQ[48]
M_DATA_B17	AN35	DDR1_DQ[17]/DDR0_DQ[49]
M_DATA_B18	AN32	DDR1_DQ[18]/DDR0_DQ[50]
M_DATA_B19	AP32	DDR1_DQ[19]/DDR0_DQ[51]
M_DATA_B20	AN34	DDR1_DQ[20]/DDR0_DQ[52]
M_DATA_B21	AP34	DDR1_DQ[21]/DDR0_DQ[53]
M_DATA_B22	AN31	DDR1_DQ[22]/DDR0_DQ[54]
M_DATA_B23	AP31	DDR1_DQ[23]/DDR0_DQ[55]
M_DATA_B24	AL29	DDR1_DQ[24]/DDR0_DQ[56]
M_DATA_B25	AM29	DDR1_DQ[25]/DDR0_DQ[57]
M_DATA_B26	AP29	DDR1_DQ[26]/DDR0_DQ[58]
M_DATA_B27	AR29	DDR1_DQ[27]/DDR0_DQ[59]
M_DATA_B28	AM28	DDR1_DQ[28]/DDR0_DQ[60]
M_DATA_B29	AL28	DDR1_DQ[29]/DDR0_DQ[61]
M_DATA_B30	AR28	DDR1_DQ[30]/DDR0_DQ[62]
M_DATA_B31	AP28	DDR1_DQ[31]/DDR0_DQ[63]
M_DATA_B32	AR12	DDR1_DQ[32]/DDR1_DQ[16]
M_DATA_B33	AP12	DDR1_DQ[33]/DDR1_DQ[17]
M_DATA_B34	AM13	DDR1_DQ[34]/DDR1_DQ[18]
M_DATA_B35	AL13	DDR1_DQ[35]/DDR1_DQ[19]
M_DATA_B36	AR13	DDR1_DQ[36]/DDR1_DQ[20]
M_DATA_B37	AP13	DDR1_DQ[37]/DDR1_DQ[21]
M_DATA_B38	AM12	DDR1_DQ[38]/DDR1_DQ[22]
M_DATA_B39	AL12	DDR1_DQ[39]/DDR1_DQ[23]
M_DATA_B40	AP10	DDR1_DQ[40]/DDR1_DQ[24]
M_DATA_B41	AR10	DDR1_DQ[41]/DDR1_DQ[25]
M_DATA_B42	AR7	DDR1_DQ[42]/DDR1_DQ[26]
M_DATA_B43	AP7	DDR1_DQ[43]/DDR1_DQ[27]
M_DATA_B44	AR9	DDR1_DQ[44]/DDR1_DQ[28]
M_DATA_B45	AP9	DDR1_DQ[45]/DDR1_DQ[29]
M_DATA_B46	AR6	DDR1_DQ[46]/DDR1_DQ[30]
M_DATA_B47	AP6	DDR1_DQ[47]/DDR1_DQ[31]
M_DATA_B48	AM10	DDR1_DQ[48]
M_DATA_B49	AL10	DDR1_DQ[49]
M_DATA_B50	AM7	DDR1_DQ[50]
M_DATA_B51	AL7	DDR1_DQ[51]
M_DATA_B52	AM9	DDR1_DQ[52]
M_DATA_B53	AL9	DDR1_DQ[53]
M_DATA_B54	AM6	DDR1_DQ[54]
M_DATA_B55	AL6	DDR1_DQ[55]
M_DATA_B56	AJ6	DDR1_DQ[56]
M_DATA_B57	AJ7	DDR1_DQ[57]
M_DATA_B58	AE6	DDR1_DQ[58]
M_DATA_B59	AE7	DDR1_DQ[59]
M_DATA_B60	AH7	DDR1_DQ[60]
M_DATA_B61	AH6	DDR1_DQ[61]
M_DATA_B62	AE7	DDR1_DQ[62]
M_DATA_B63	AE6	DDR1_DQ[63]
AR25	DDR1_ECC[0]	
AR26	DDR1_ECC[1]	
AM25	DDR1_ECC[2]	
AP25	DDR1_ECC[3]	
AP26	DDR1_ECC[4]	
AP25	DDR1_ECC[5]	
AL25	DDR1_ECC[6]	
AL26	DDR1_ECC[7]	

CPU1B

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SKYLAKE-S  
Rev.0.7

## DDR CHANNEL B

2 OF 12

LGA 1151 SOCKET

DDR1\_CKP[0] AM20 >>> CK\_M\_CH1\_0\_DP 12  
DDR1\_CKN[0] AM21 >>> CK\_M\_CH1\_0\_DN 12  
DDR1\_CKP[1] AP22 >>> CK\_M\_CH1\_1\_DP 12  
DDR1\_CKN[1] AP21 >>> CK\_M\_CH1\_1\_DN 12  
DDR1\_CKP[2] AN20  
DDR1\_CKN[2] AN21  
DDR1\_CKP[3] AP19  
DDR1\_CKN[3] AP20

DDR1\_CKE[0] AY29 >>> M\_SCKE\_B0 12  
DDR1\_CKE[1] AY29 >>> M\_SCKE\_B1 12  
DDR1\_CKE[2] AW29  
DDR1\_CKE[3] AU29

DDR1\_CS#[0] AP17 >>> M\_SCS\_B\_N0 12  
DDR1\_CS#[1] AN15 >>> M\_SCS\_B\_N1 12  
DDR1\_CS#[2] AN17  
DDR1\_CS#[3] AM15

DDR1\_ODT[0] AL16 >>> M\_ODT\_B0 12  
DDR1\_ODT[1] AL16 >>> M\_ODT\_B1 12  
DDR1\_ODT[2] AP15  
DDR1\_ODT[3] AL15

DDR1\_RAS#/DDR1\_CAB[3]/DDR1\_MA[16] AN18 M MAA\_B16 >>> M\_MAA\_B[0..16] 12  
DDR1\_WE#/DDR1\_CAB[2]/DDR1\_MA[14] AL17 M MAA\_B14  
DDR1\_CAS#/DDR1\_CAB[1]/DDR1\_MA[15] AP16 M MAA\_B15

DDR1\_BA[0]/DDR1\_CAB[4]/DDR1\_BA[0] AL18 >>> M\_SBS\_B0 12  
DDR1\_BA[1]/DDR1\_CAB[5]/DDR1\_BA[1] AM18 >>> M\_SBS\_B1 12  
DDR1\_BA[2]/DDR1\_CAA[5]/DDR1\_BG[0] AW28 >>> M\_BG\_CH1\_0 12

DDR1\_MA[0]/DDR1\_CAB[9]/DDR1\_MA[0] AL19 M MAA\_B0 >>> M\_MAA\_B[0..16] 12  
DDR1\_MA[1]/DDR1\_CAB[8]/DDR1\_MA[1] AL22 M MAA\_B1  
DDR1\_MA[2]/DDR1\_CAB[5]/DDR1\_MA[2] AM22 M MAA\_B2  
DDR1\_MA[3] AM23 M MAA\_B3  
DDR1\_MA[4] AP23 M MAA\_B4  
DDR1\_MA[5] AW23 M MAA\_B5  
DDR1\_MA[6] AW26 M MAA\_B6  
DDR1\_MA[7] AW26 M MAA\_B7  
DDR1\_MA[8] AU26 M MAA\_B8  
DDR1\_MA[9] AW27 M MAA\_B9  
DDR1\_MA[10] AP18 M MAA\_B10  
DDR1\_MA[11] AU27 M MAA\_B11  
DDR1\_MA[12] AV27 M MAA\_B12  
DDR1\_MA[13] AR15 M MAA\_B13

DDR1\_MA[5]/DDR1\_CAA[0]/DDR1\_MA[5]  
DDR1\_MA[6]/DDR1\_CAA[2]/DDR1\_MA[6]  
DDR1\_MA[7]/DDR1\_CAA[4]/DDR1\_MA[7]  
DDR1\_MA[8]/DDR1\_CAA[3]/DDR1\_MA[8]  
DDR1\_MA[9]/DDR1\_CAA[1]/DDR1\_MA[9]  
DDR1\_MA[10]/DDR1\_CAB[7]/DDR1\_MA[10]  
DDR1\_MA[11]/DDR1\_CAA[7]/DDR1\_MA[11]  
DDR1\_MA[12]/DDR1\_CAA[6]/DDR1\_MA[12]  
DDR1\_MA[13]/DDR1\_CAB[0]/DDR1\_MA[13]  
DDR1\_MA[14]/DDR1\_CAA[9]/DDR1\_BG[1]  
DDR1\_MA[15]/DDR1\_CAA[8]/DDR1\_ACT#

DDR1\_PAR AL20 >>> DDR\_CH1\_PAR 12  
DDR1\_ALERT# AY25 >>> DDR\_CH1\_ALERT\_N 12

DDR1\_QOSN[0]/DDR0\_QOSN[2] AF34 >>> M\_QOS\_B\_DN0 12  
DDR1\_QOSN[1]/DDR0\_QOSN[3] AK33 >>> M\_QOS\_B\_DN1 12  
DDR1\_QOSN[2]/DDR0\_QOSN[6] AN33 >>> M\_QOS\_B\_DN2 12  
DDR1\_QOSN[3]/DDR0\_QOSN[7] AN29 >>> M\_QOS\_B\_DN3 12  
DDR1\_QOSN[4]/DDR1\_QOSN[2] AN13 >>> M\_QOS\_B\_DN4 12  
DDR1\_QOSN[5]/DDR1\_QOSN[3] AR8 >>> M\_QOS\_B\_DN5 12  
DDR1\_QOSN[6] AM8 >>> M\_QOS\_B\_DN6 12  
DDR1\_QOSN[7] AG6 >>> M\_QOS\_B\_DN7 12

DDR1\_QOSP[0]/DDR0\_QOSP[2] AF35 >>> M\_QOS\_B\_DP0 12  
DDR1\_QOSP[1]/DDR0\_QOSP[3] AL33 >>> M\_QOS\_B\_DP1 12  
DDR1\_QOSP[2]/DDR0\_QOSP[6] AP33 >>> M\_QOS\_B\_DP2 12  
DDR1\_QOSP[3]/DDR0\_QOSP[7] AN28 >>> M\_QOS\_B\_DP3 12  
DDR1\_QOSP[4]/DDR1\_QOSP[2] AN12 >>> M\_QOS\_B\_DP4 12  
DDR1\_QOSP[5]/DDR1\_QOSP[3] AP8 >>> M\_QOS\_B\_DP5 12  
DDR1\_QOSP[6] AL8 >>> M\_QOS\_B\_DP6 12  
DDR1\_QOSP[7] AG7 >>> M\_QOS\_B\_DP7 12

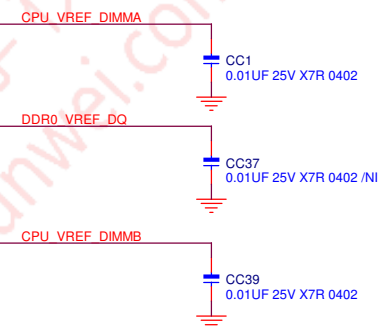
DDR1\_QOSP[8] AN25  
DDR1\_QOSP[9] AN26

DDR\_VREF\_CA AB40 CPU VREF DIMMA >>> CPU\_VREF\_DIMMA 11  
DDR0\_VREF\_DQ AC40 DDR0 VREF DQ >>> CPU\_VREF\_DIMMA 11  
DDR1\_VREF\_DQ AC39 CPU VREF DIMMB >>> CPU\_VREF\_DIMMB 12

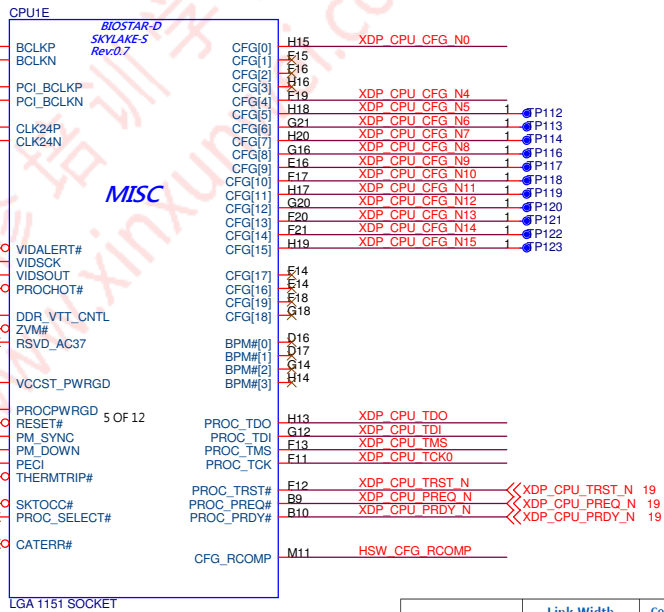
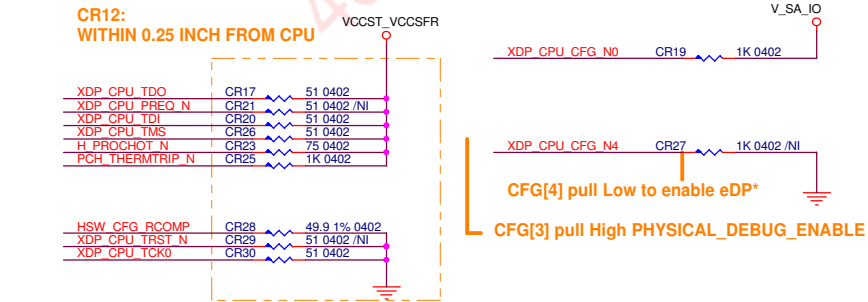
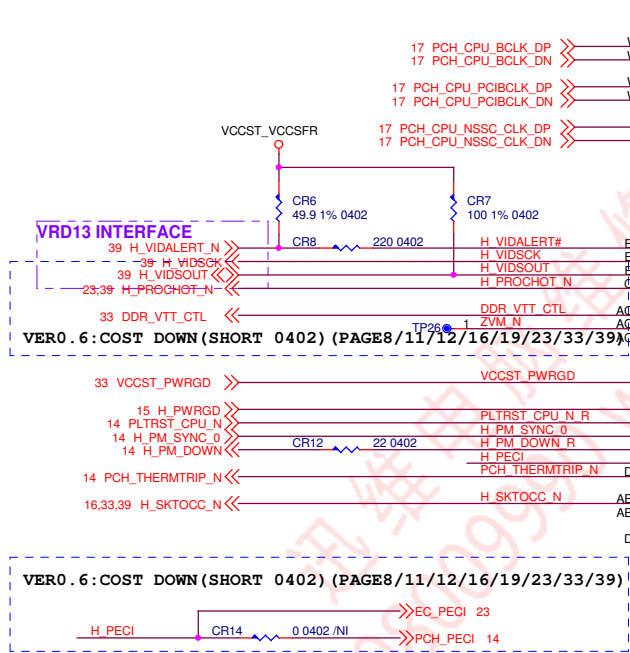
M\_QOS\_B\_DP[0..7] >>> M\_QOS\_B\_DP[0..7] 12

M\_QOS\_B\_DN[0..7] >>> M\_QOS\_B\_DN[0..7] 12

VER0.60:DDR3 CHANGE DDR4(PAGE6/7/11/12)

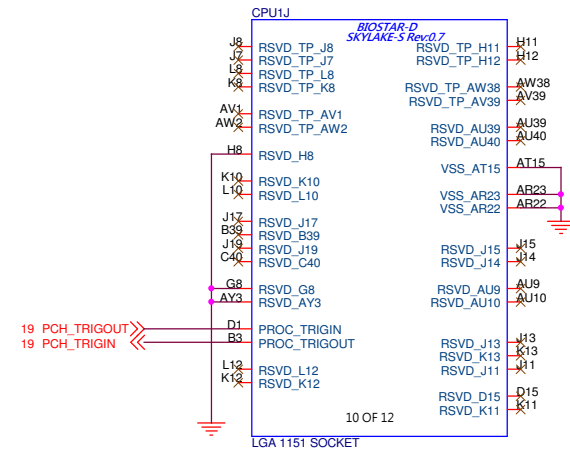


Title CPU DDR3 CHANNEL B	
Size B	Document Number IH11M-MHS
Date: Friday, January 08, 2016	Sheet 7 of 42
Rev 6.0	




Bifurcation	Link Width			Config. Signals		
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]
1x16	x16	N/A	N/A	1	1	1
1x16 Reversed	x16	N/A	N/A	1	1	0
2x8	x8	x8	N/A	1	0	1
2x8 Reversed	x8	x8	N/A	1	0	0
1x8+2x4	x8	x4	x4	0	0	1
1x8+2x4 Reversed	x8	x4	x4	0	0	0

CFG[19:0]	<p><b>Configuration Signals:</b> The CFG signals have a default value of '1'. If not terminated on the board, refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p><b>CFG[0]:</b> Stall reset sequence after PCU PLL lock until de-asserted.</p> <ul style="list-style-type: none"><li>1 = (Default) Normal Operation; 0 = stall.</li><li><b>CFG[1]:</b> Reserved configuration lane.</li><li><b>CFG[2]:</b> PCI Express® Static x16 Lane Reversal.</li><li>1 = Normal operation.</li><li>0 = Lane numbers reversed.</li><li><b>CFG[3]:</b> Reserved configuration lane.</li><li><b>CFG[4]:</b> eDP enable.</li><li>1 = Enabled.</li><li>0 = Disabled.</li><li><b>CFG[5]:</b> PCI Express® Bifurcation.</li><li>00 = 1 x8, 2 x8 PCI Express®.</li><li>01 = reserved.</li><li>10 = 2 x8 PCI Express®.</li><li>11 = 1 x16 PCI Express®.</li><li><b>CFG[7]:</b> PEG Training.</li><li>1 = (Default) PEG Training immediately following RESET# de-assertion.</li><li>0 = PEG Wait for BIOS for training.</li><li><b>CFG[10-15]:</b> Reserved configuration lanes.</li></ul>
-----------	---



CFG	HIGH	LOW	STRAP DESCRIPTION
0	NORMAL	STALL	EAR
1	NORMAL	PCHLESS	PCHLESS MODE
2	NORMAL	REVERSE	PEG_LANE_REVERSAL
3	ENABLE	DISABLE	PHYSICAL_DEBUG_ENABLE
4	DISABLE	ENABLE	DP PRESENCE
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET_N	BIOS REQ	PEG_DEFER_TRAINING
8	DISABLE	ENABLE	CFG_UNLOCK
9	PRESENT	NOT PRESENT	SVID NOT PRESENT
10	ACTIVATE	DEACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DMI_AC_COUPLED
12	PMSYNC 2.0	LEGACY	PMSYNC LEGACY
13	SYNC	ASYN	PMSYNC ASYN MODE
14	RESERVED		
15	RESERVED		

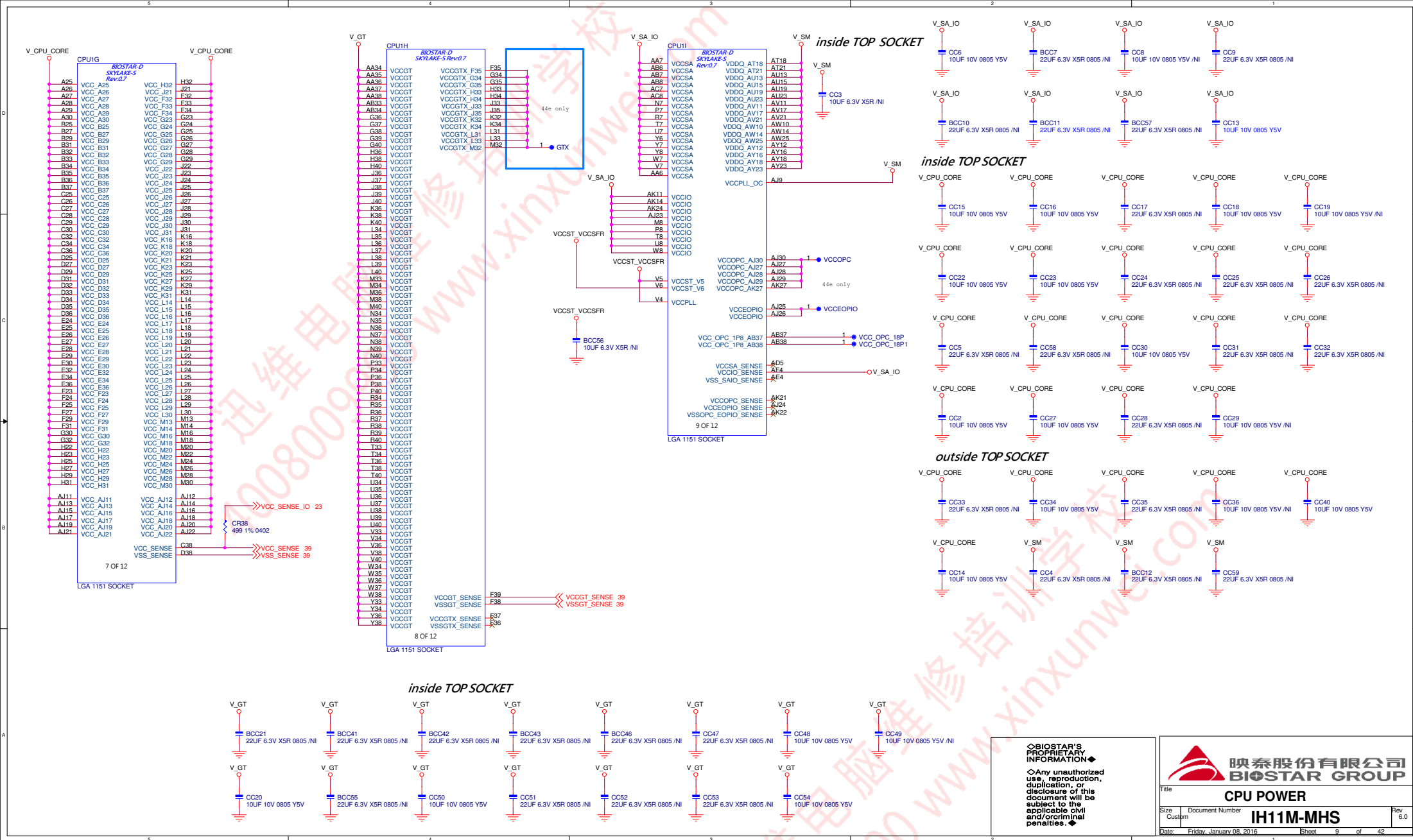
ALL PINS HAVE INTERNAL PULL-UPS

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**CPU MISC**

Size	Document Number	Rev
Custpm	IH11M-MHS	6.0
Date:	Friday, January 08, 2016	Sheet 8 of 42





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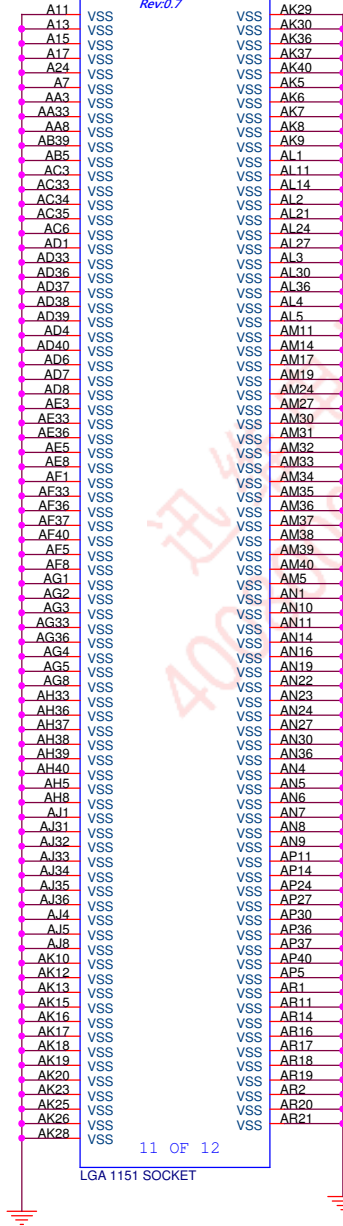
Rev 6.0

Sheet 9 of 42

CPU POWER

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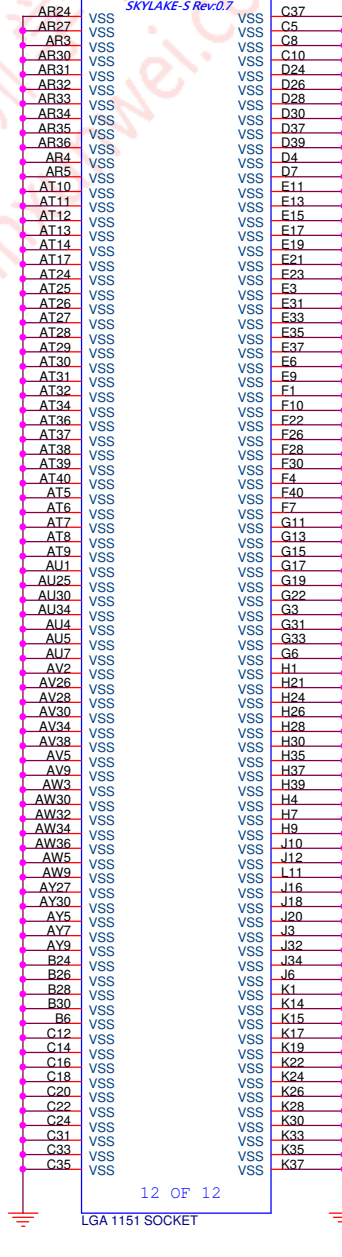
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Rev.0.7

11 OF 12

LGA 1151 SOCKET

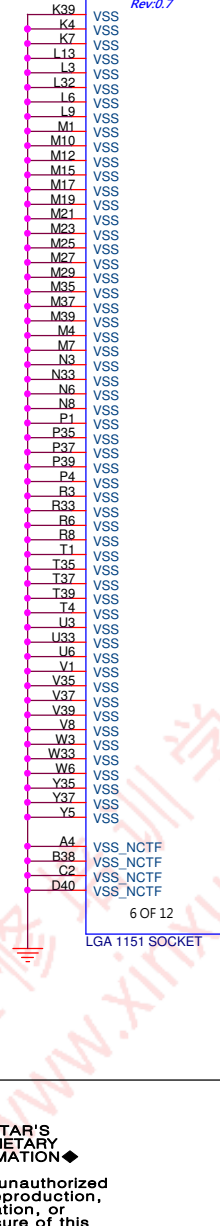
CPU1L

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SKYLAKE-S Rev.0.7

12 OF 12

LGA 1151 SOCKET

CPU1F

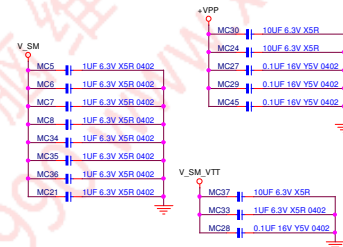
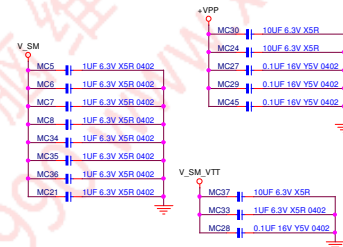
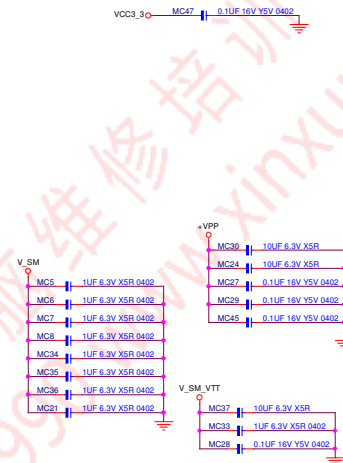
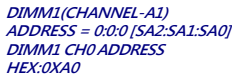
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SKYLAKE-S  
Rev.0.7

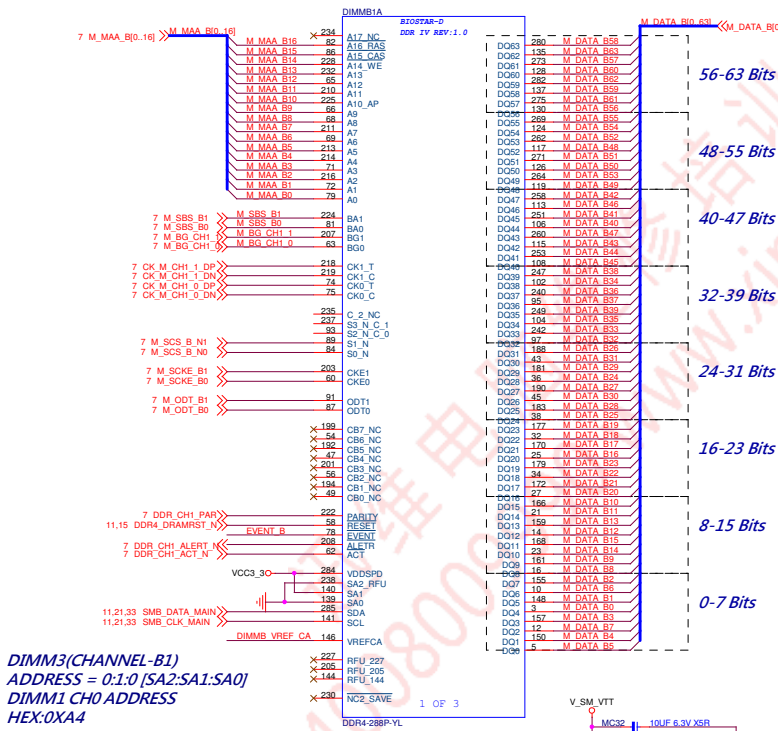
6 OF 12

LGA 1151 SOCKET

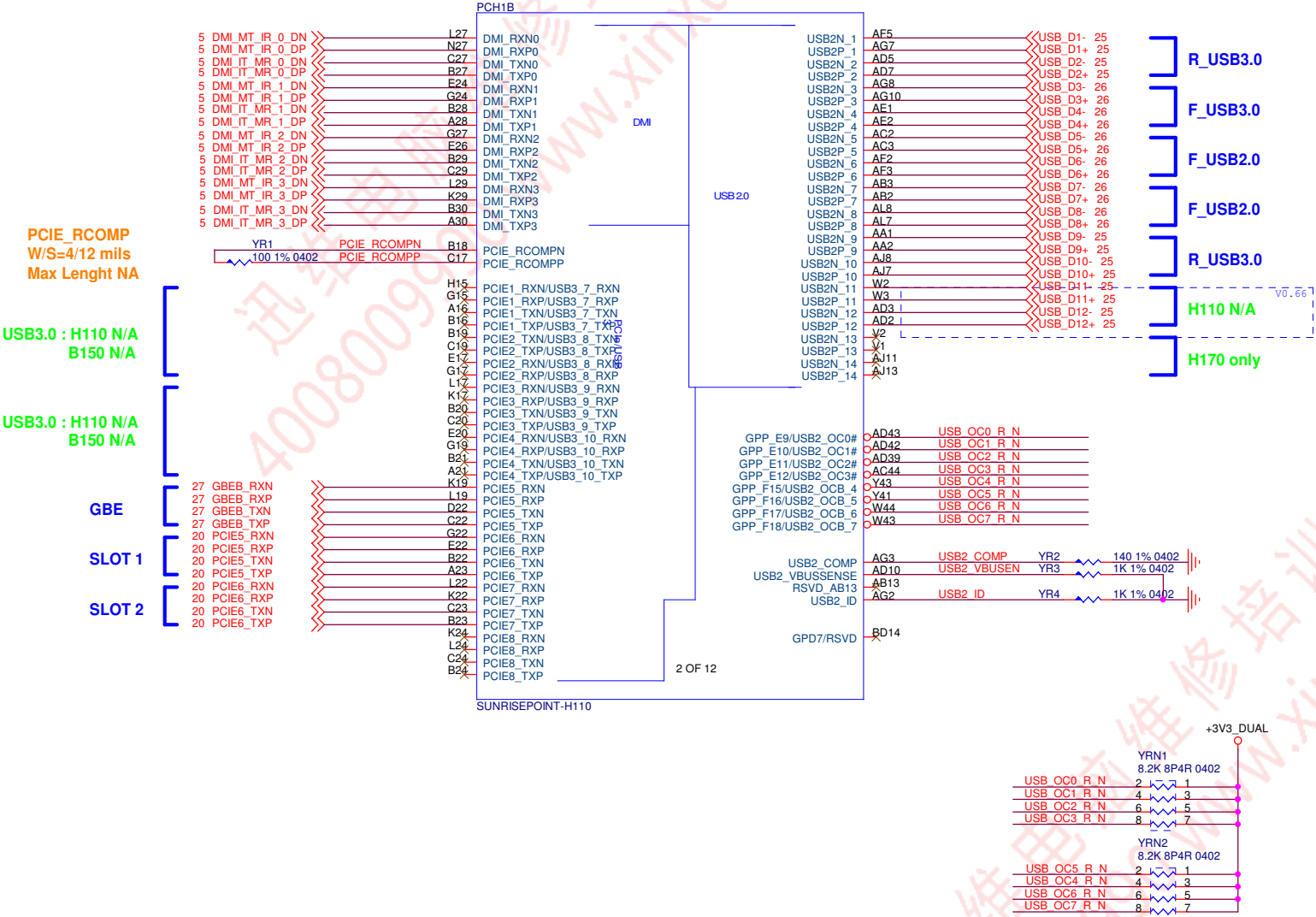
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Size	Document Number	IH11M-MHS	
B		Rev	6.0
Date:	Friday, January 08, 2016	Sheet	10 of 42





PCH PART: Y+Reference



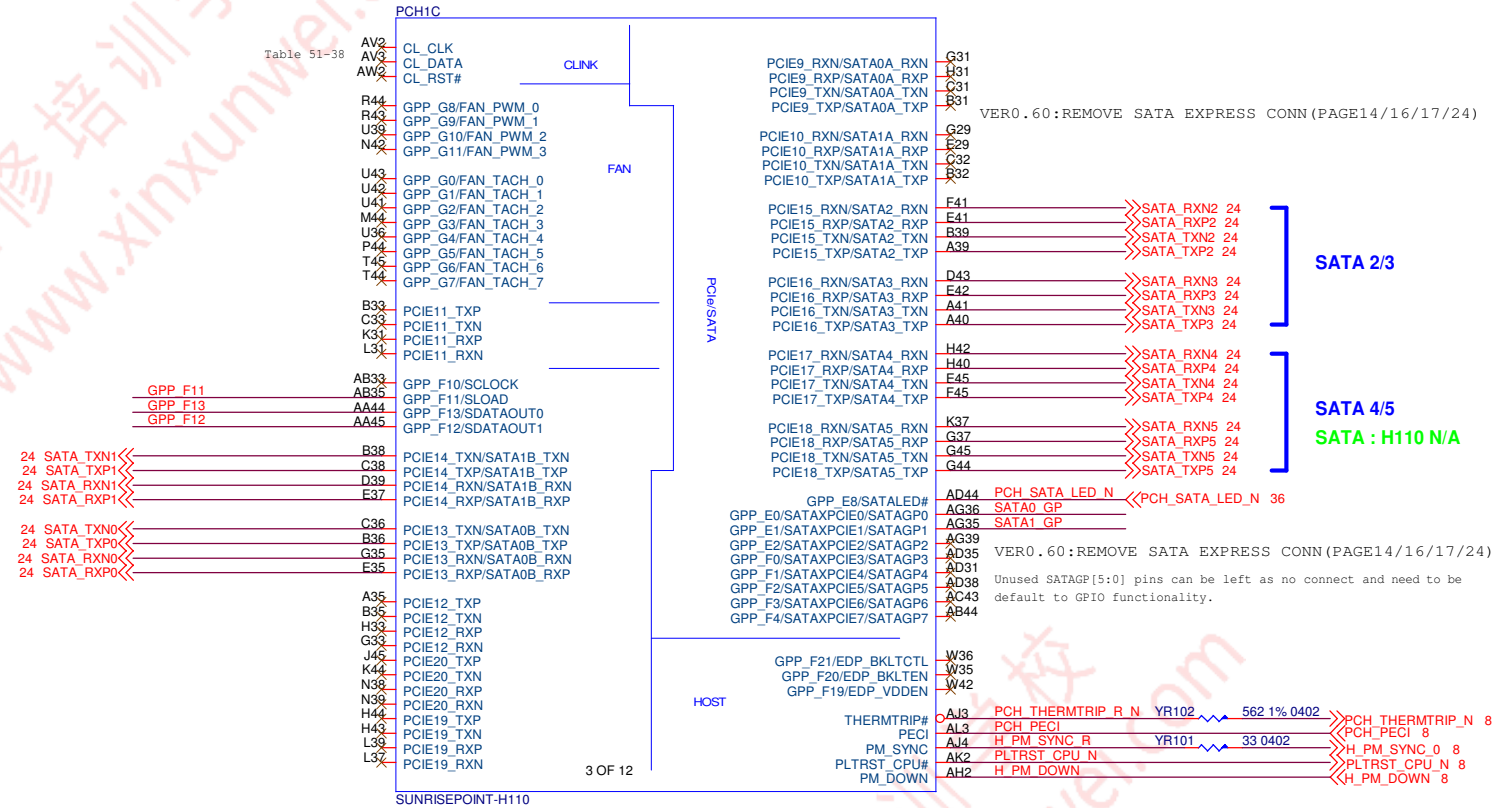
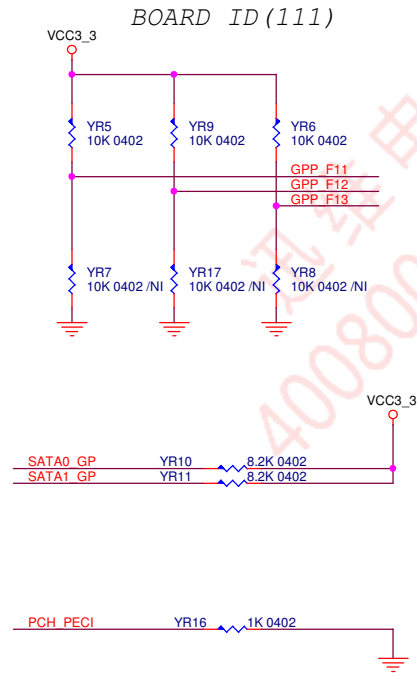
Title **PCH DMI/PCIe/USB**

Size B Document Number **IH11M-MHS** Rev 6.0

Date: Friday, January 08, 2016 Sheet 13 of 42



# PCH PART: Y+Reference



GbE can be mapped into one of the PCIe Ports 4-5, Port 9, and Ports 12-13.

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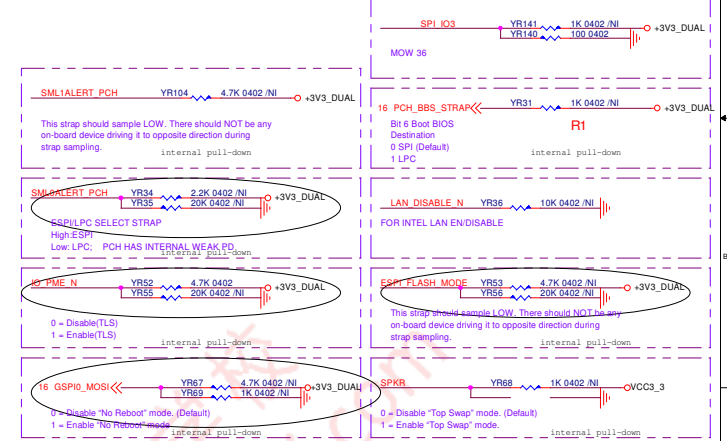
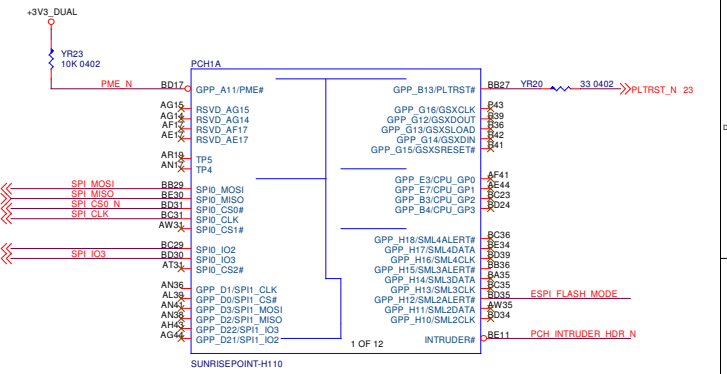
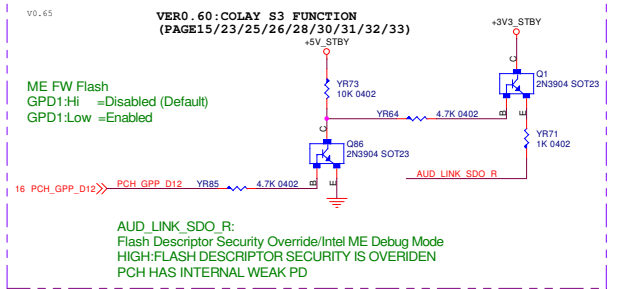
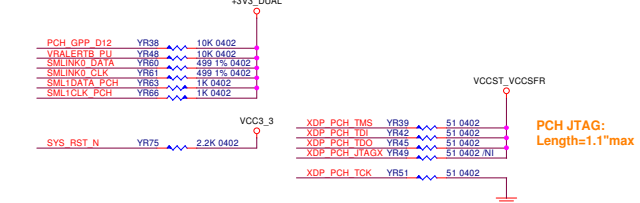
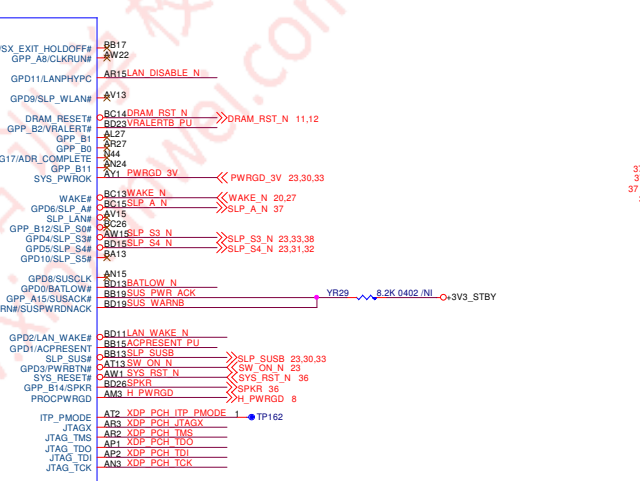
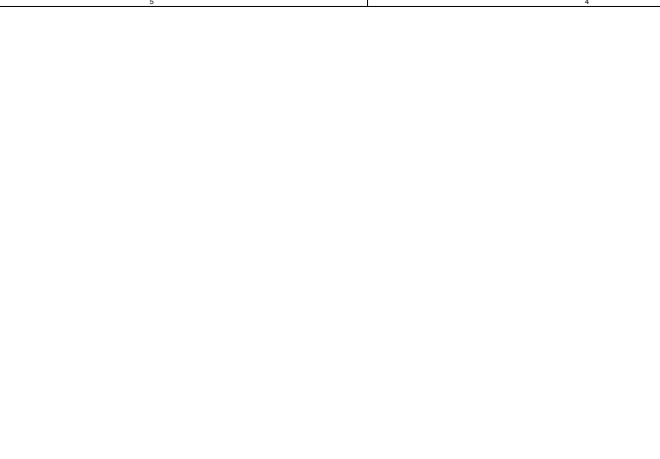
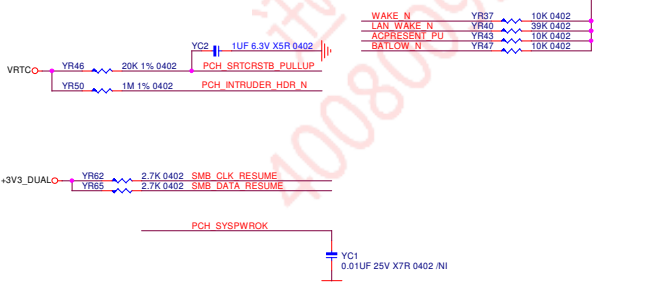
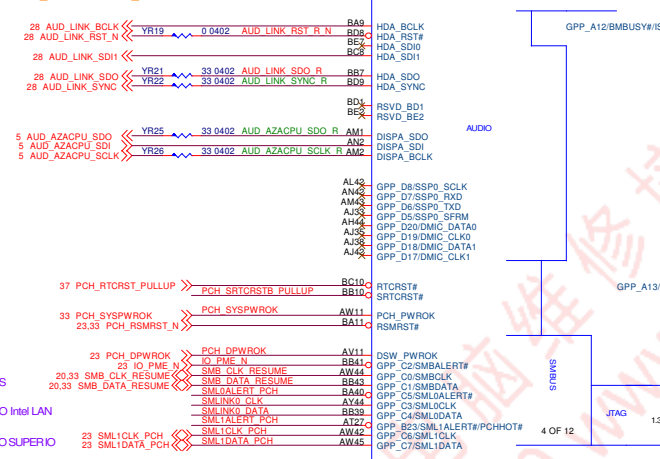


Title PCH CLINK/SATA/CPU HOST

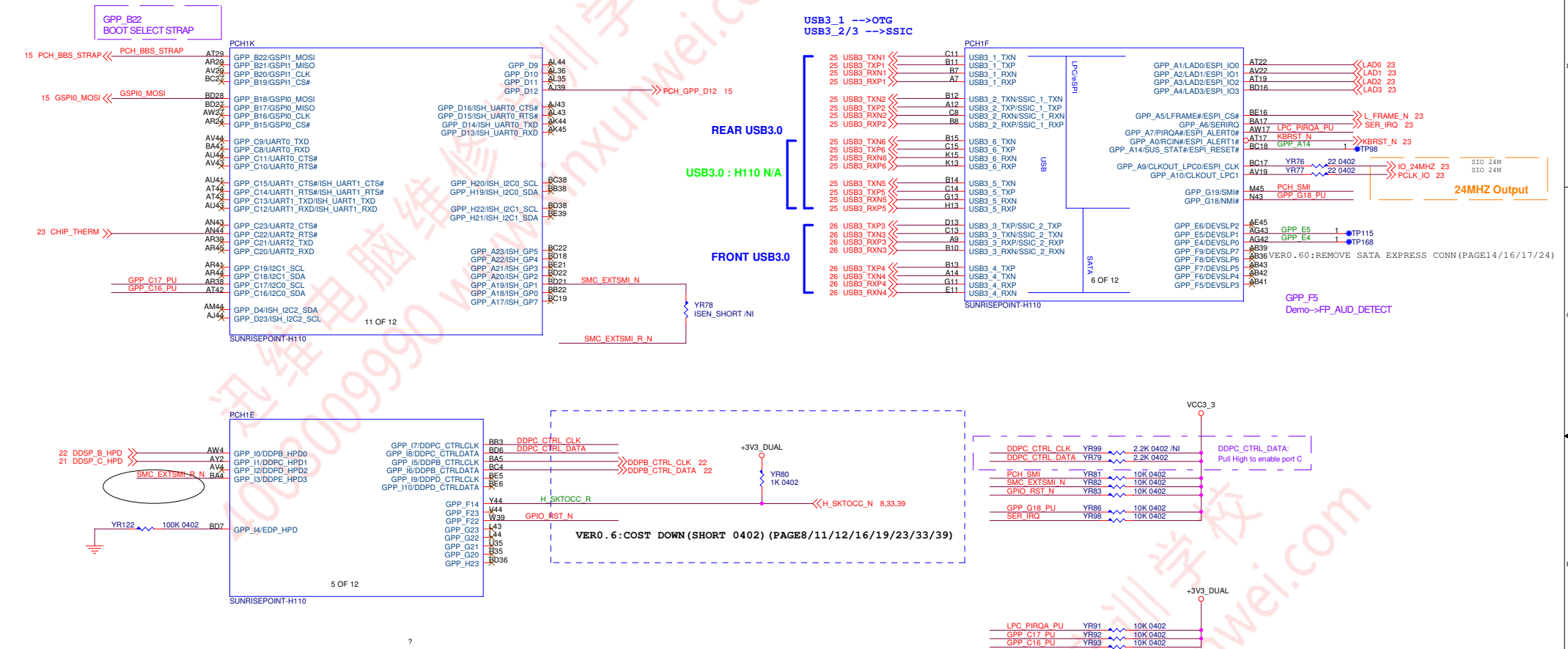
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Date: Friday, January 08, 2016 Sheet 14 of 42



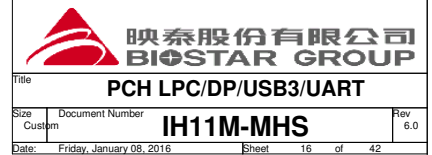


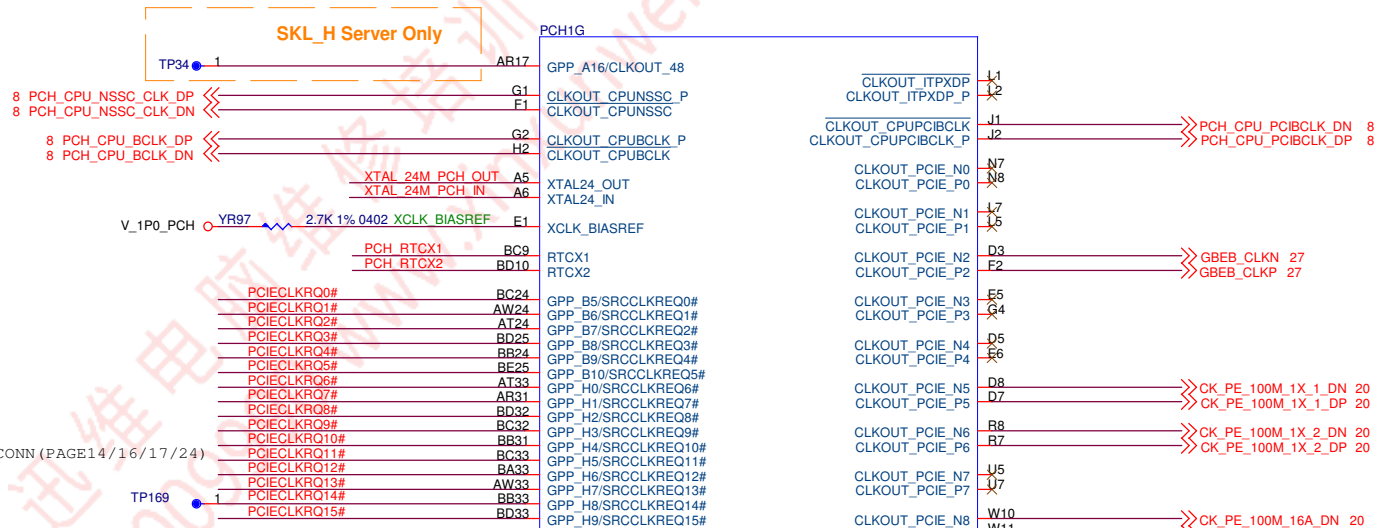
## PCH PART: Y+Reference



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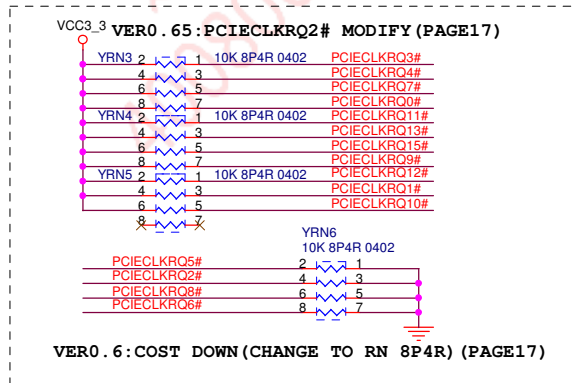
RTL 8111H

PCIE X1

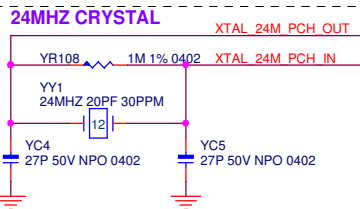
PCIE X1

PCIE X16

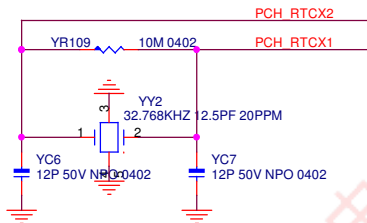
VER0.60:REMOVE SATA EXPRESS CONN (PAGE14/16/17/24)




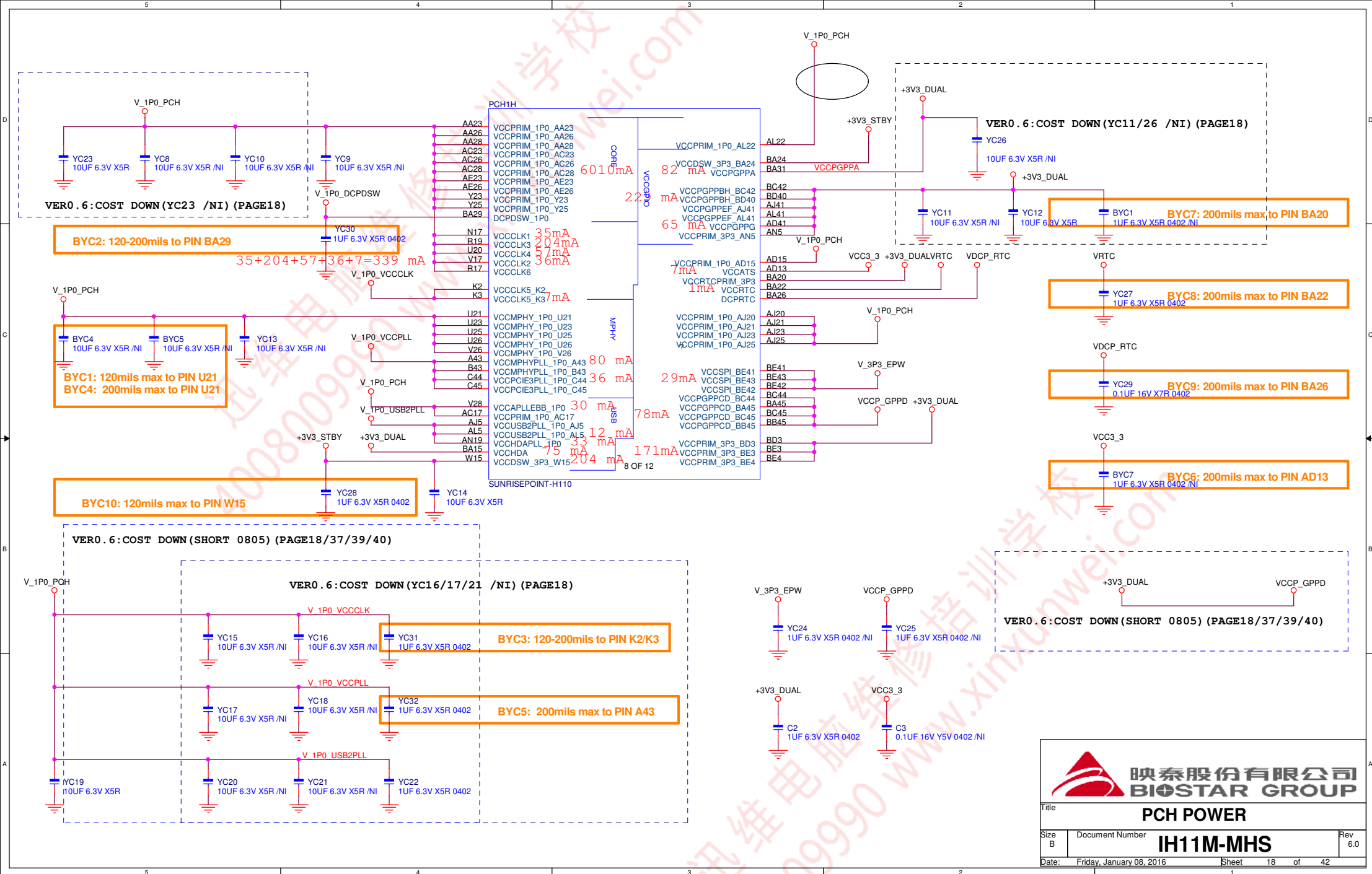
VER0.6: COST DOWN (CHANGE TO RN 8P4R) (PAGE17)

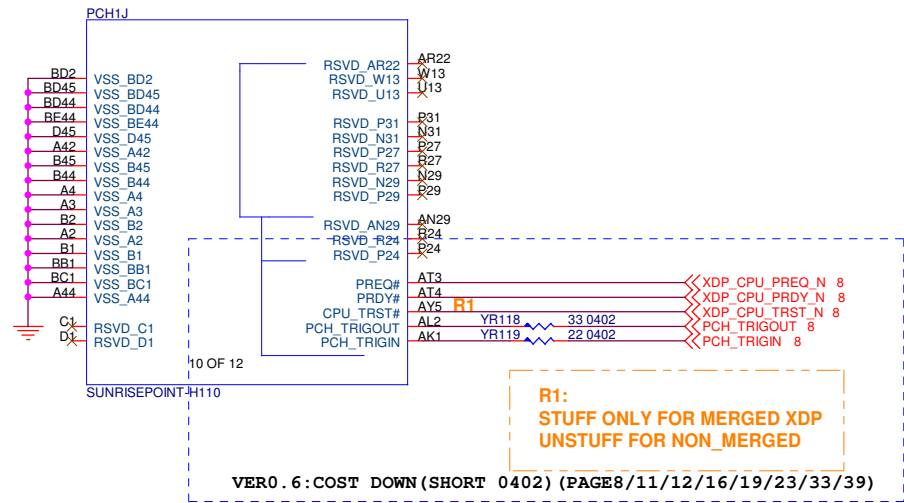
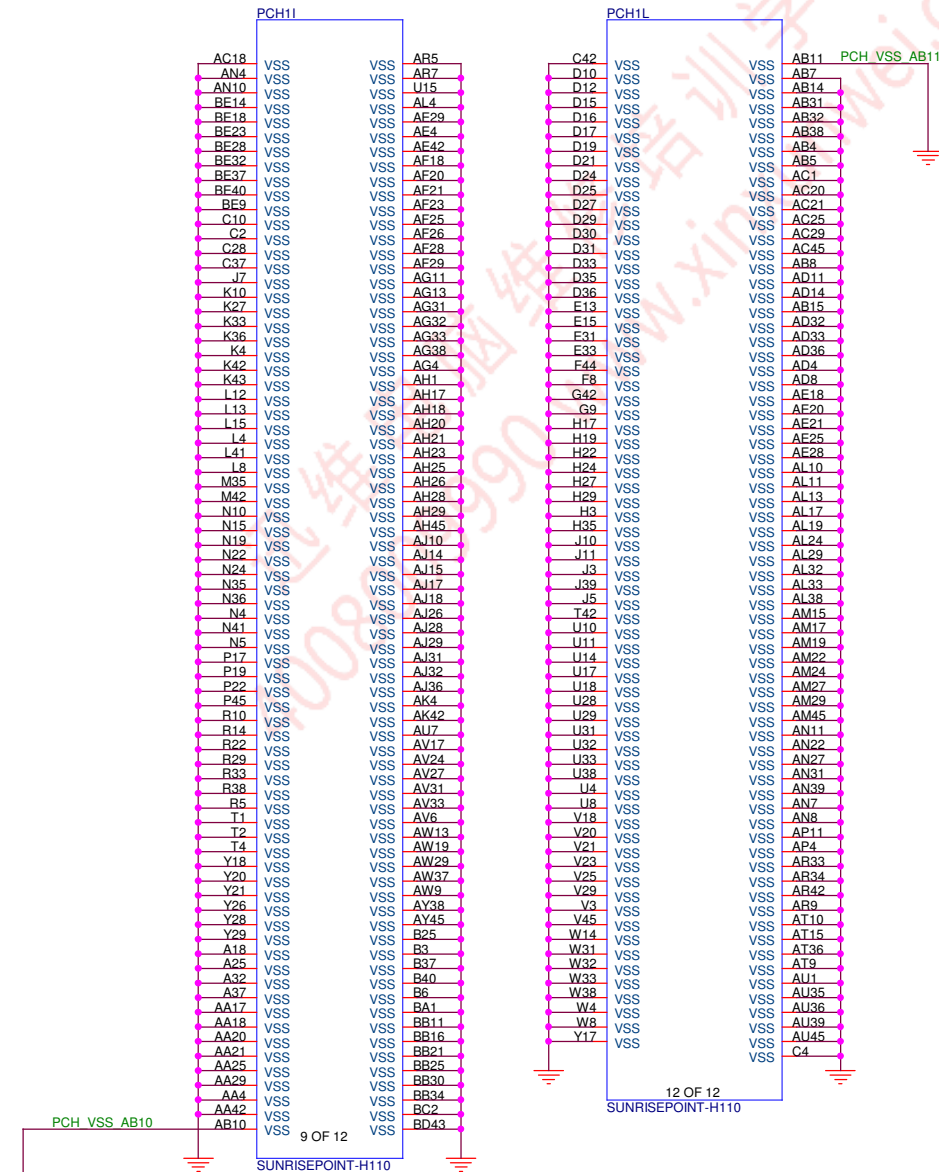


**RTC CRYSTAL**




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Title <b>PCH CLOCK BUFFER</b>			
Size B	Document Number	<b>IH11M-MHS</b>	Rev 6.0
Date:	Friday, January 08, 2016	Sheet 17	of 42





R1:  
STUFF ONLY FOR MERGED XDP  
UNSTUFF FOR NON\_MERGED

VER0.6:COST DOWN(SHORT 0402) (PAGE8/11/12/16/19/23/33/39)



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Date:

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Sheet

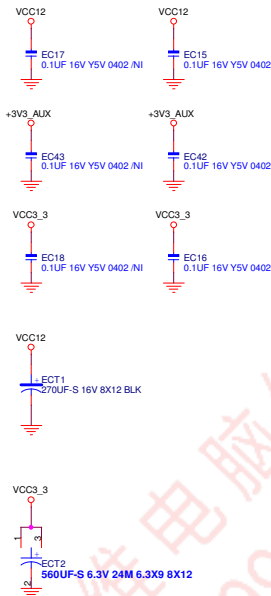
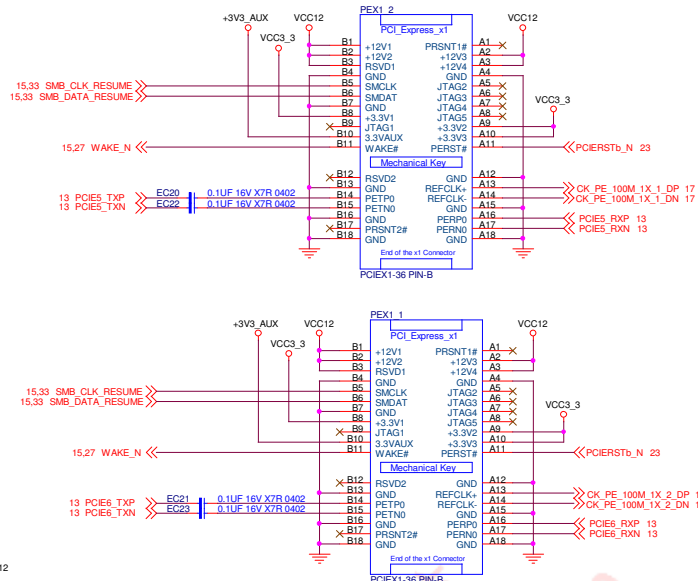
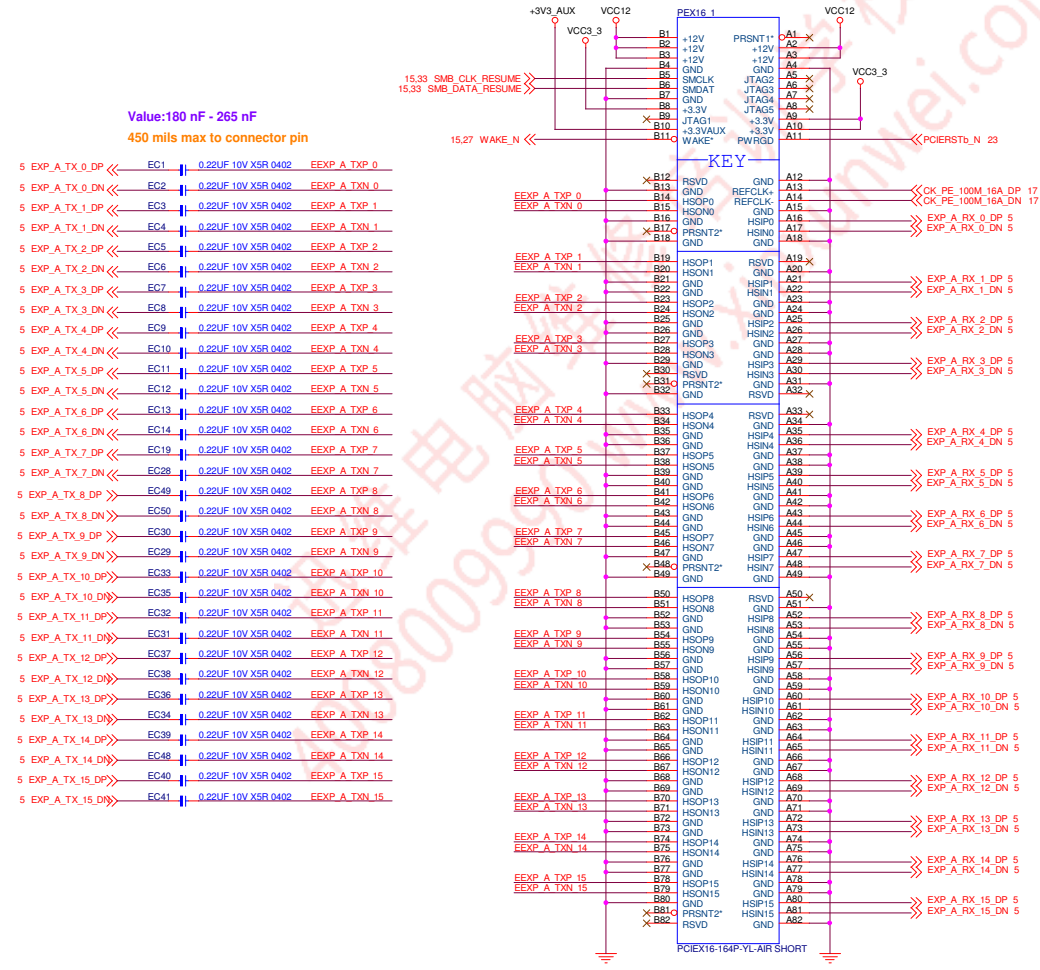
19

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42

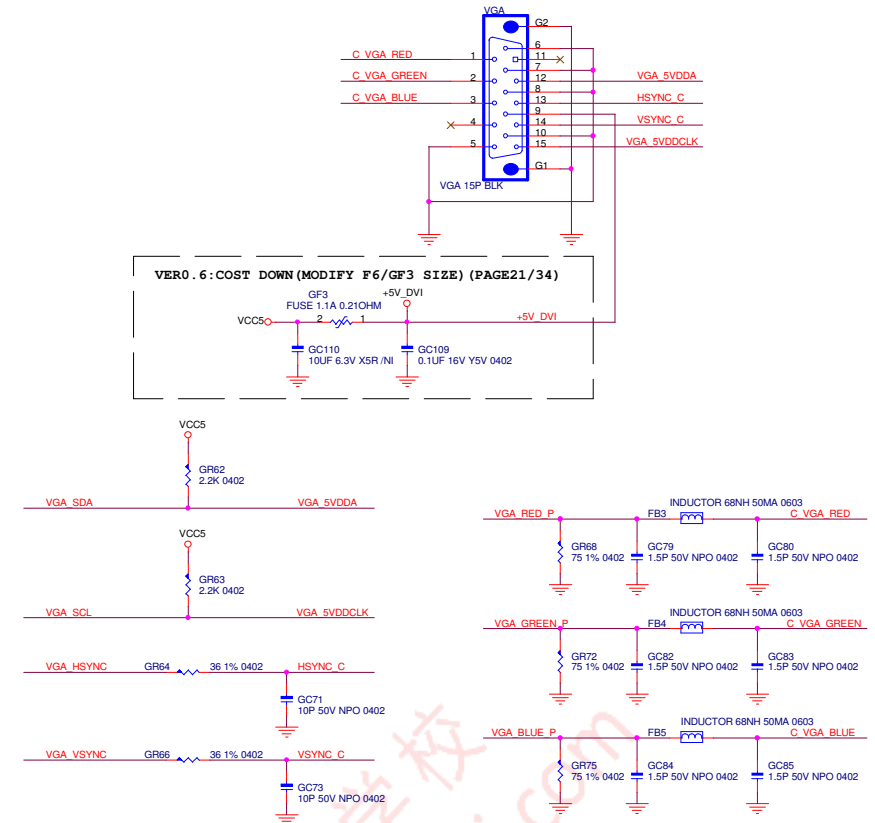
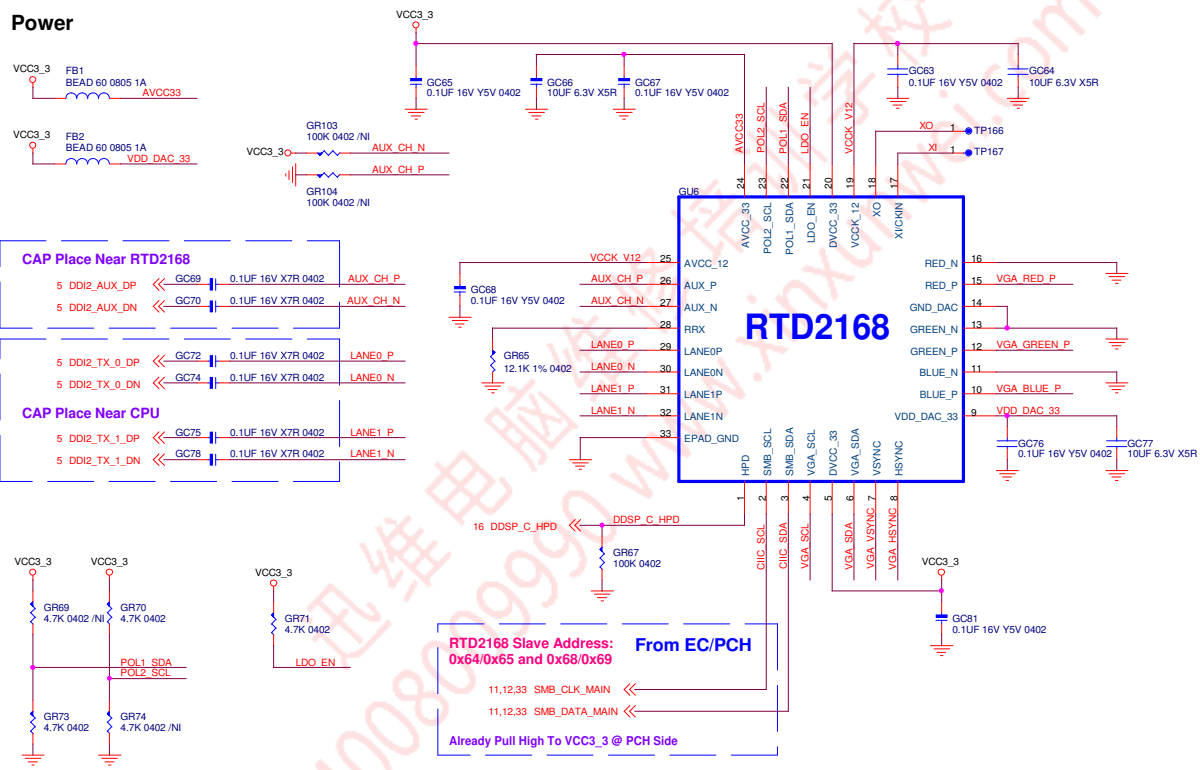


# SLOT PART: E+Reference





## Power



### Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	<b>EEPROM MODE</b>

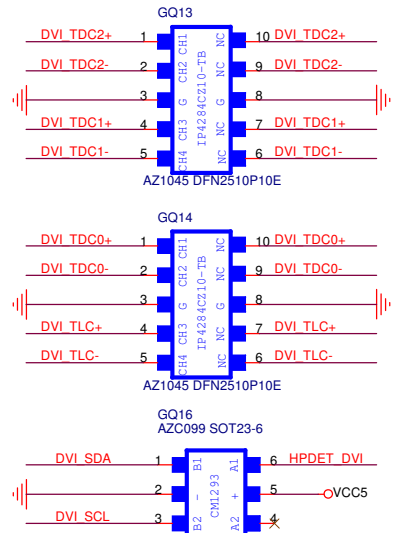
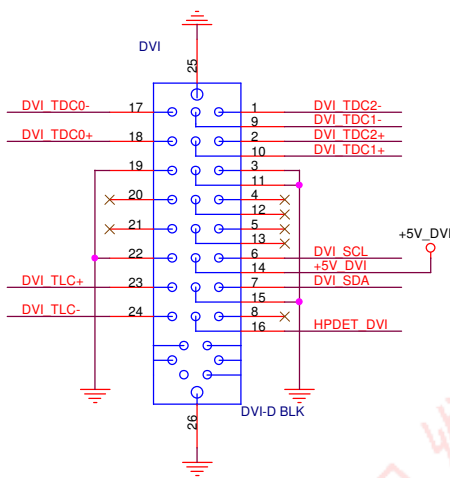
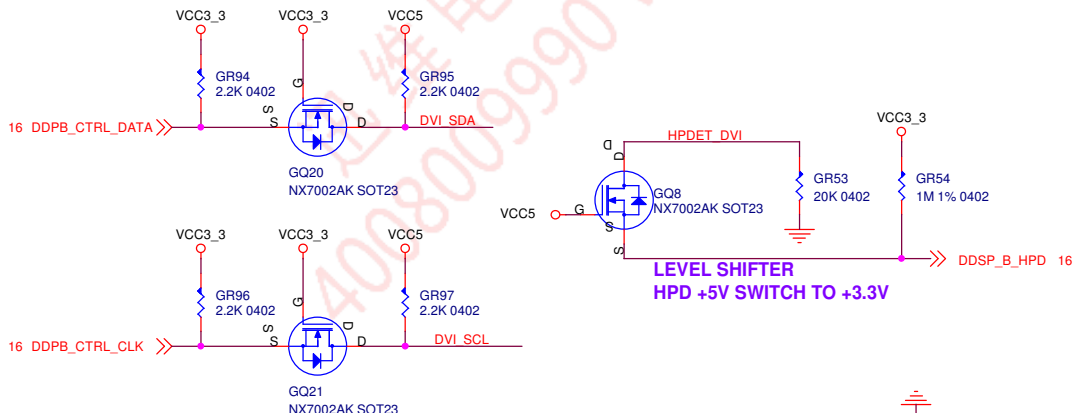
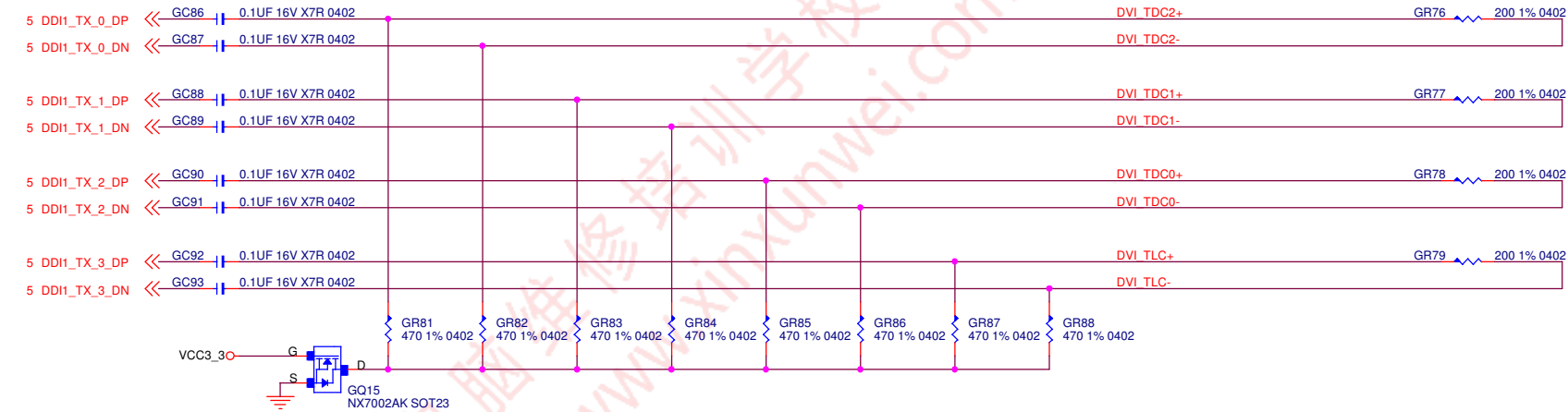
### Embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	<b>VCCK_V12 from Embedded LDO</b>


Table 12 Power consumption by using embedded LDO and embedded clock source

Active Resolution / Standby	DP Config.	Min	Type	Max	Unit
1280x800x60(74.25-MHz)	1-Lane	-	400	450	mW
1600x900x60(103-MHz)	1-Lane	-	420	480	mW
1920x1080x60(148-MHz)	2-Lane	-	480	595	mW
Stand-by mode	-	-	7.5	8	mW



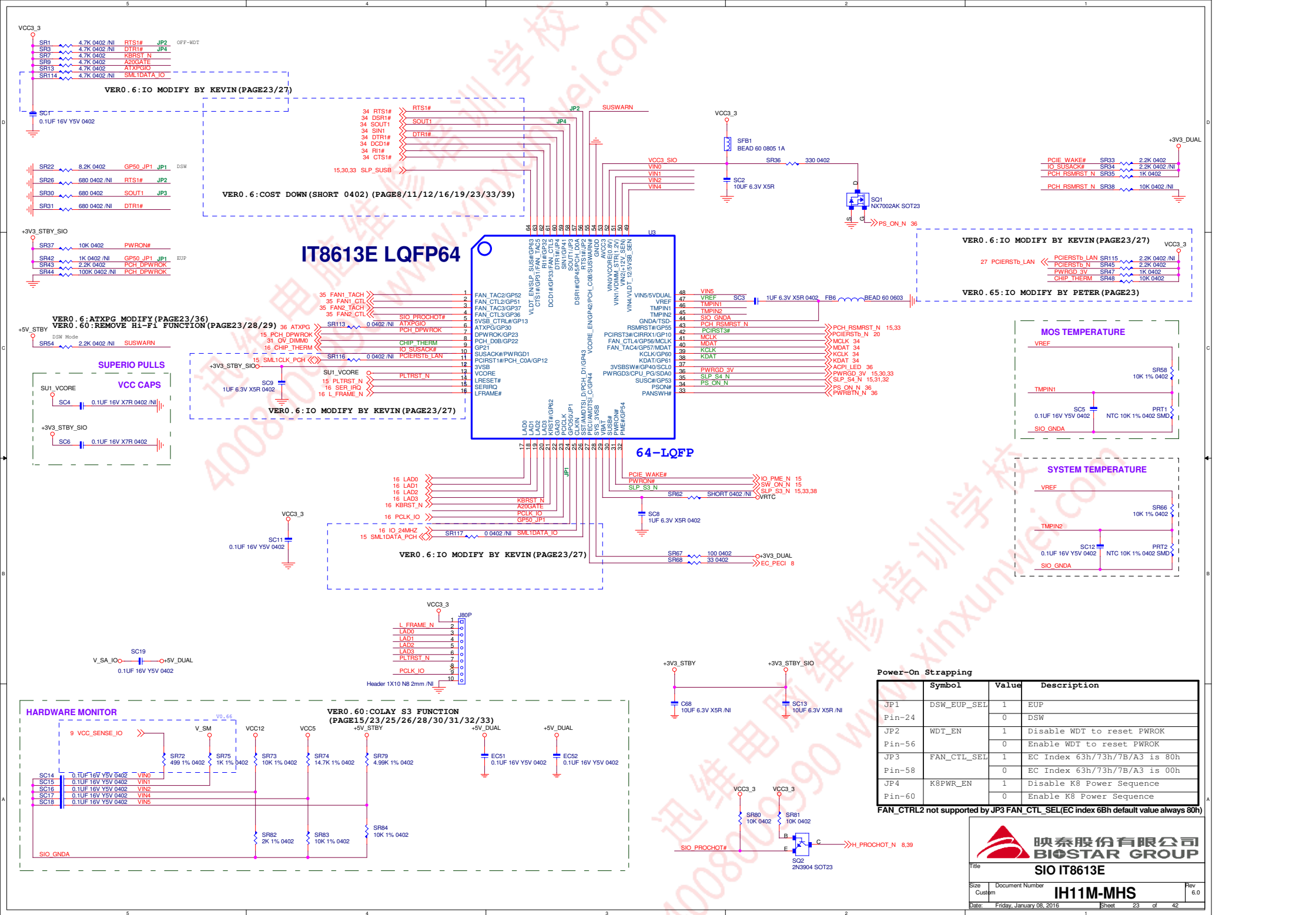


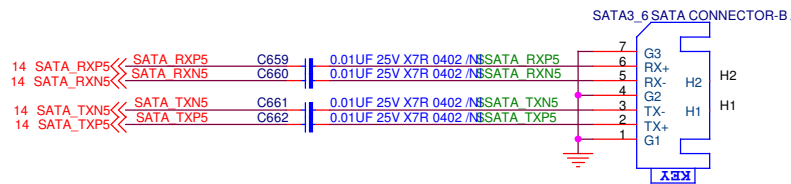
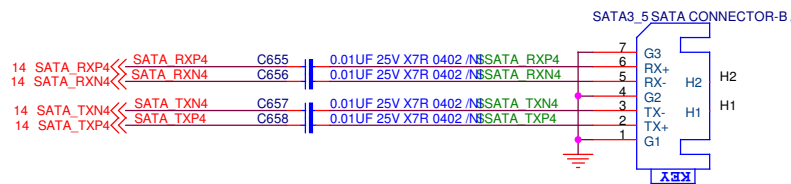
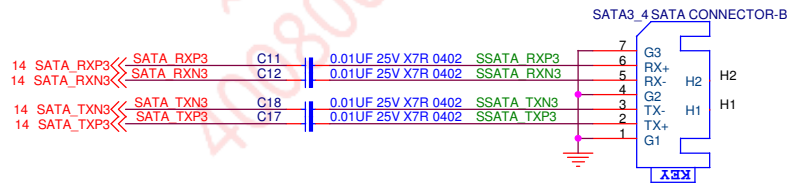
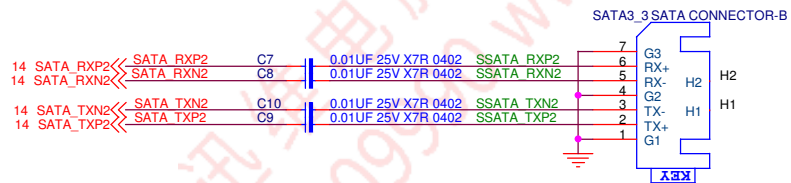
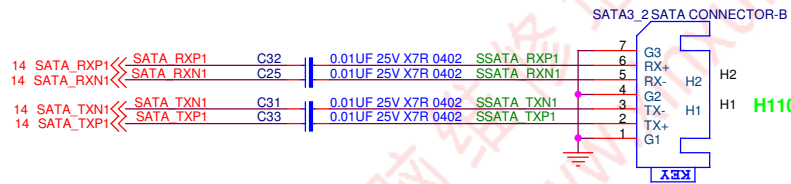
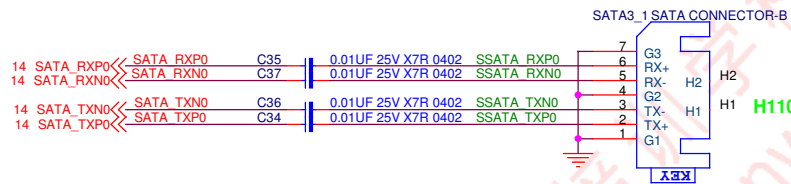
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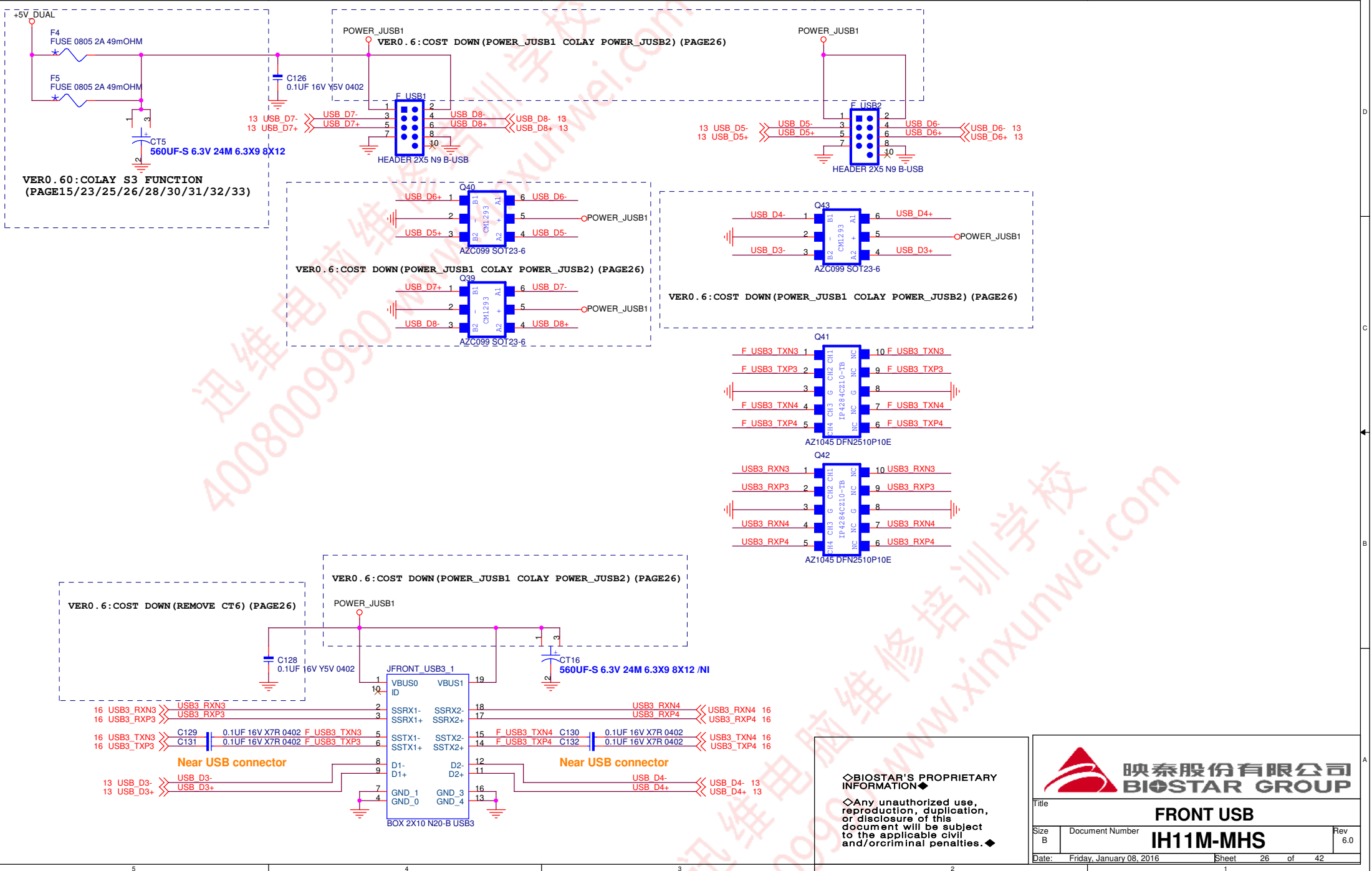


VER0.65:NEW ADD SATA CONN(PAGE14/24)


VER0.60:REMOVE SATA EXPRESS CONN(PAGE14/16/17/24)

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		SATA EXPRESS	
Size B	Document Number	IH11M-MHS	
Date: Friday, January 08, 2016		Sheet	24 of 42
		Rev	6.0

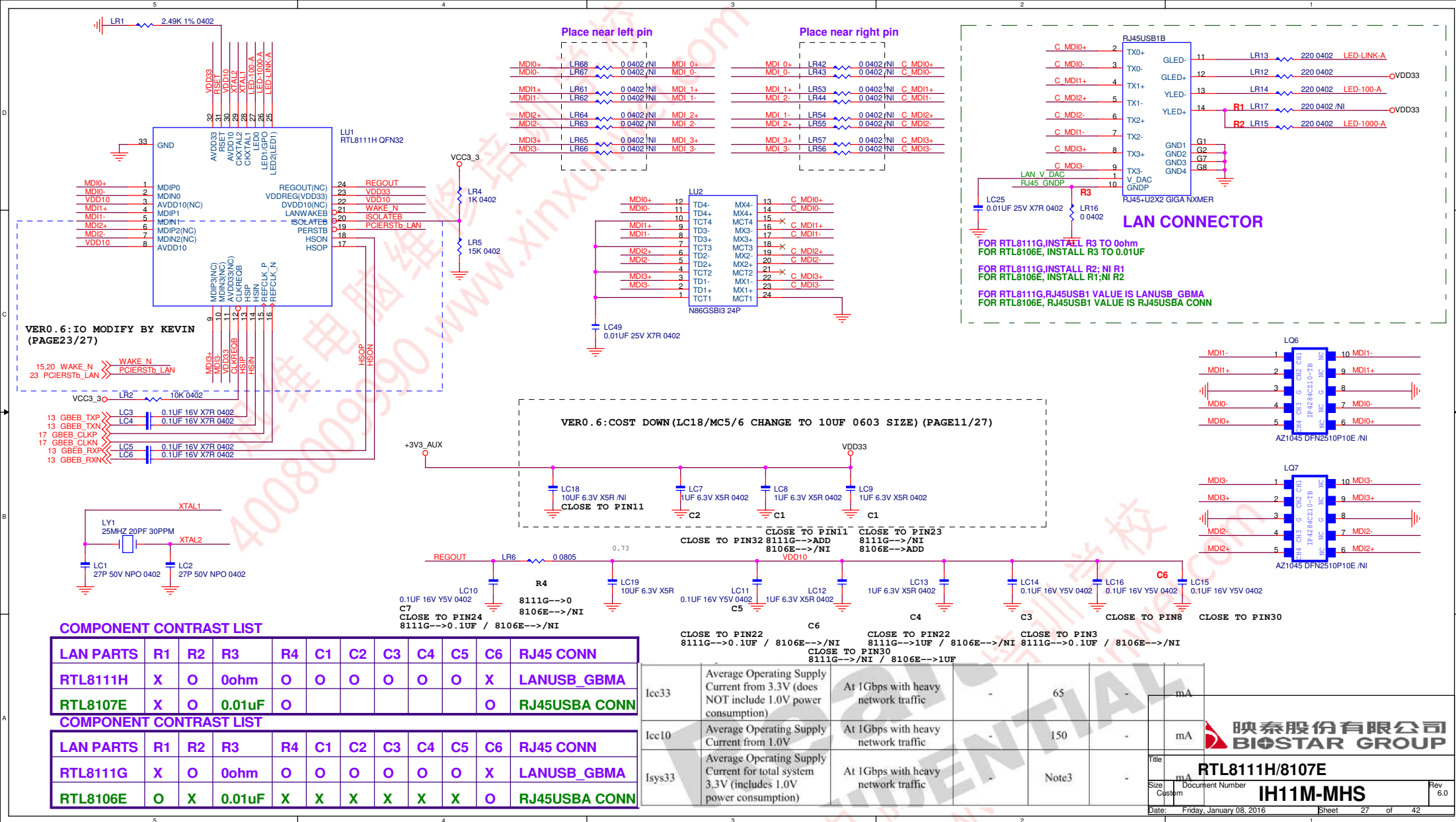


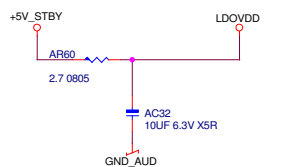


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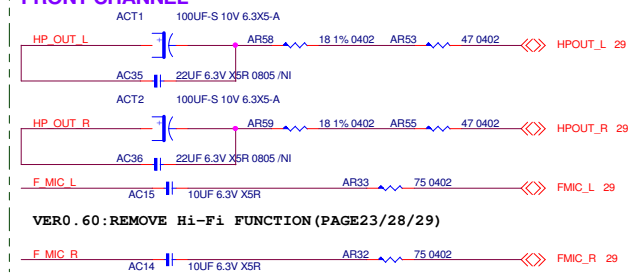






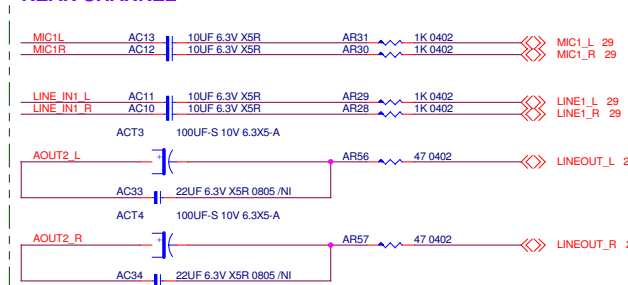
VER0.60:COLAY S3 FUNCTION  
(PAGE15/23/25/26/28/30/31/32/33)

FRONT CHANNEL



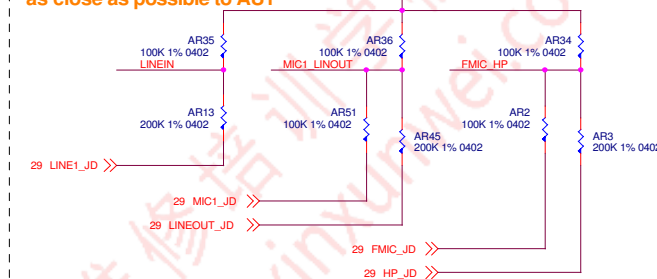
VER0.60:REMOVE Hi-Fi FUNCTION (PAGE23/28/29)

## REAR CHANNEL



## JD Group

- as close as possible to AU1



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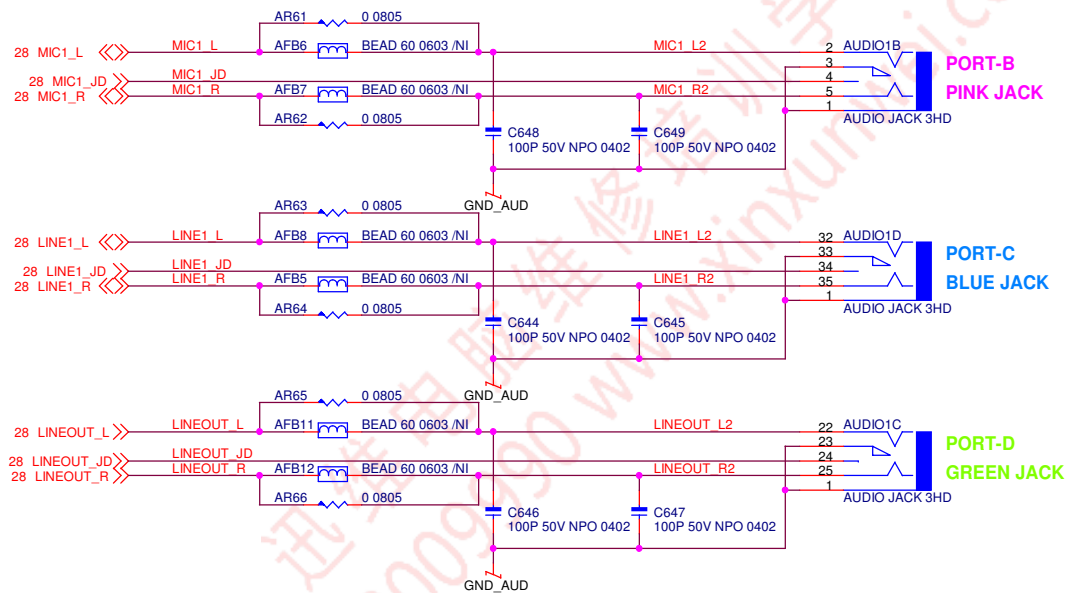
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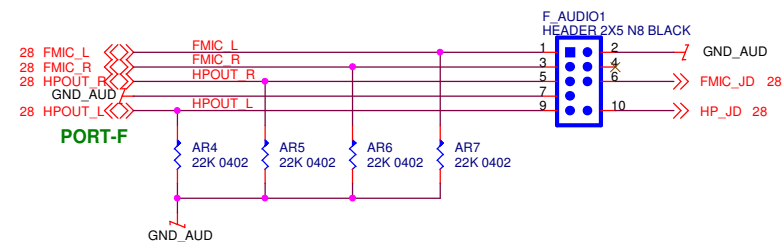
Title	<b>AUDIO CODEC ALC887</b>
-------	---------------------------

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----------------	-------------------------------------	------------

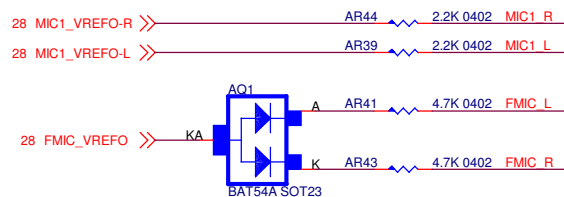
Date: Friday, January 08, 2016 Sheet 28 of 42



## FRONT AUDIO HEADER

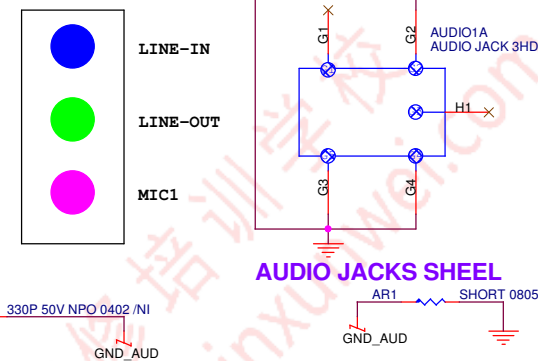


## MIC VREF



## SPDIF CONNECTOR

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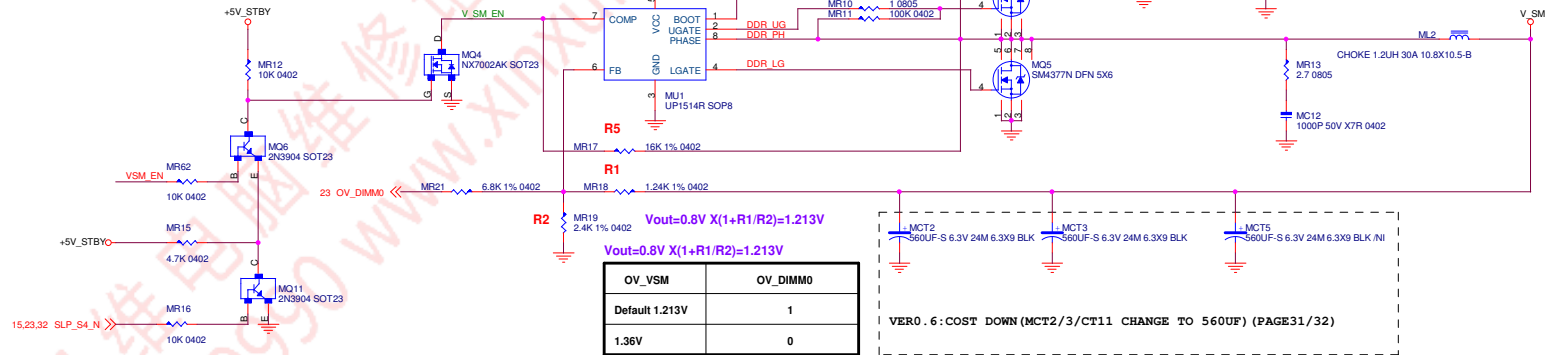
Date: Friday, January 08, 2016 Sheet 29 of 42



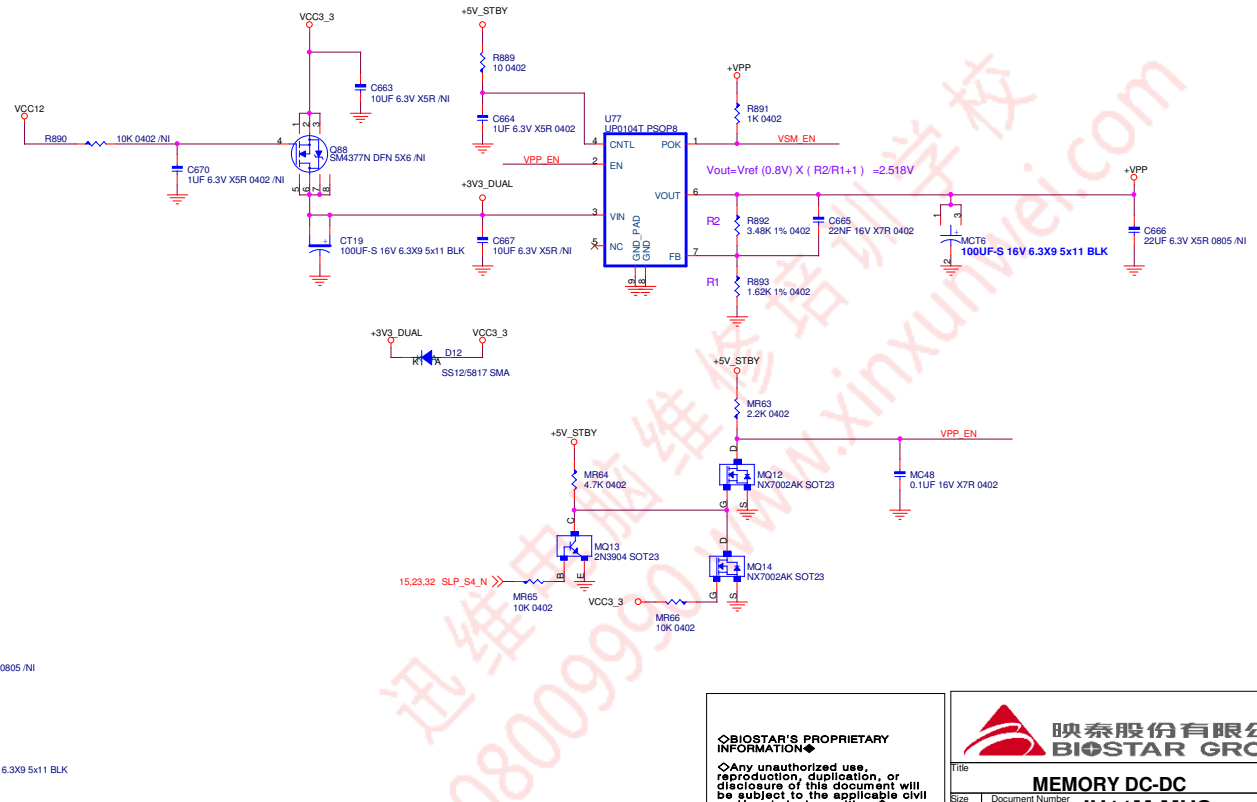
## MEMORY PART:M+Reference

VER0.60:COLAY S3 FUNCTION  
(PAGE15/23/25/26/28/30/31/32/33)

S3-->R1  
NO S3--> /NI



DDR OVER VOLTAGE TABLE

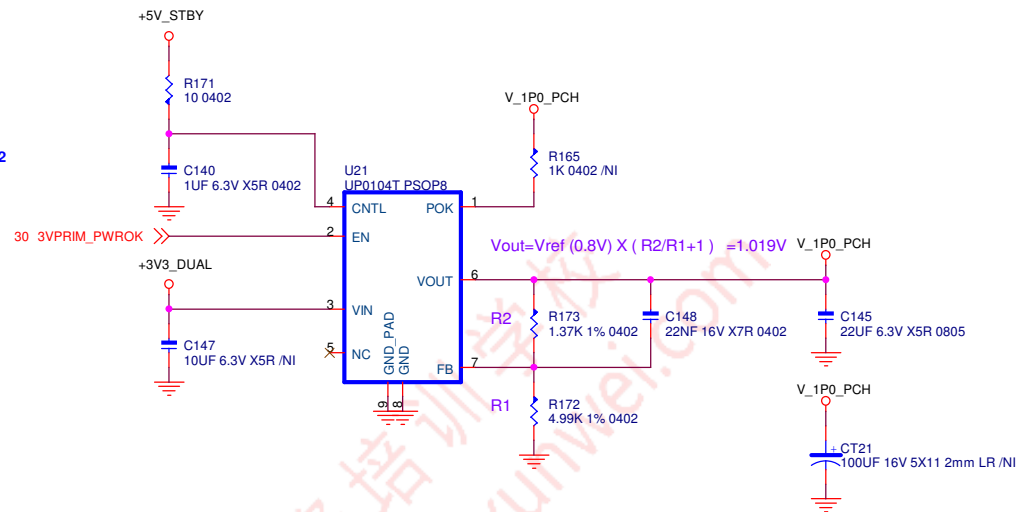
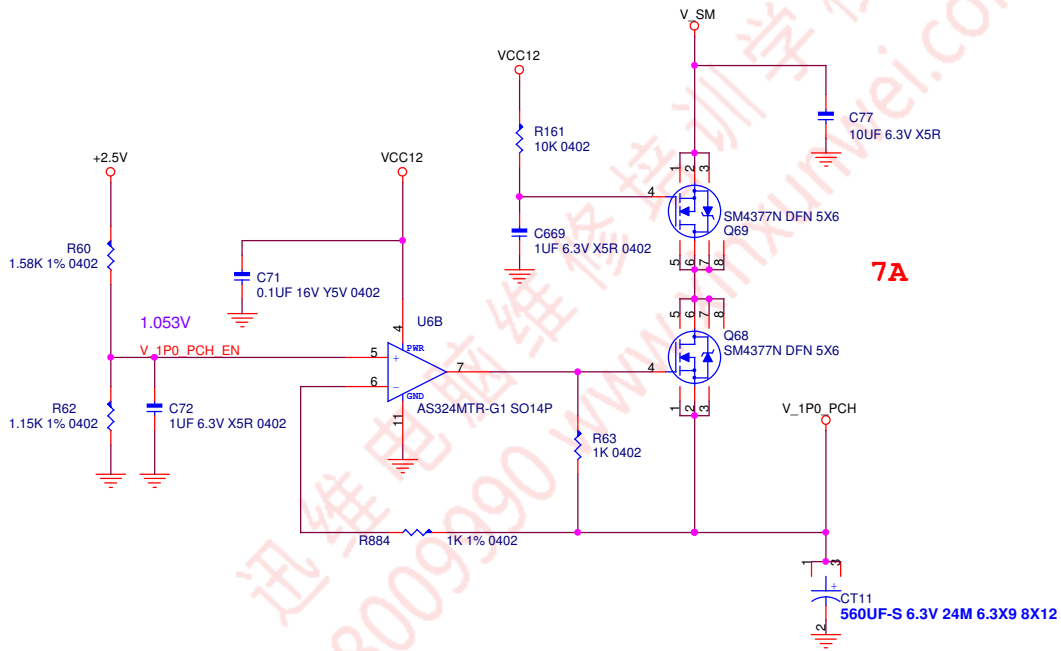


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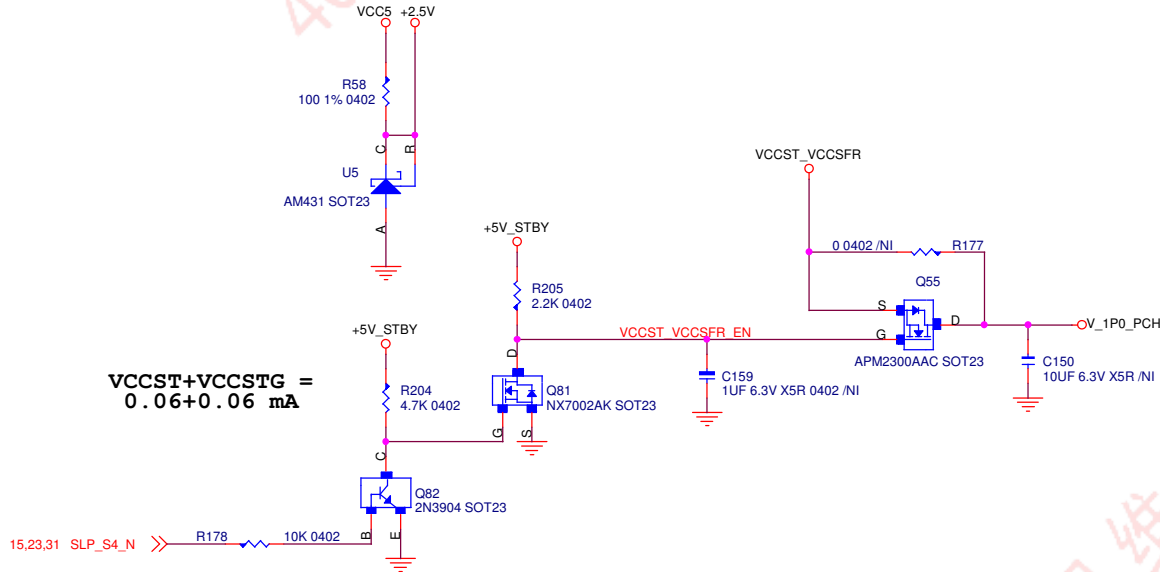
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Size	Document Number	IH11M-MHS
Date	Friday, January 08, 2016	Sheet 31 of 42



$$VCCST+VCCSTG = 0.06+0.06 \text{ mA}$$



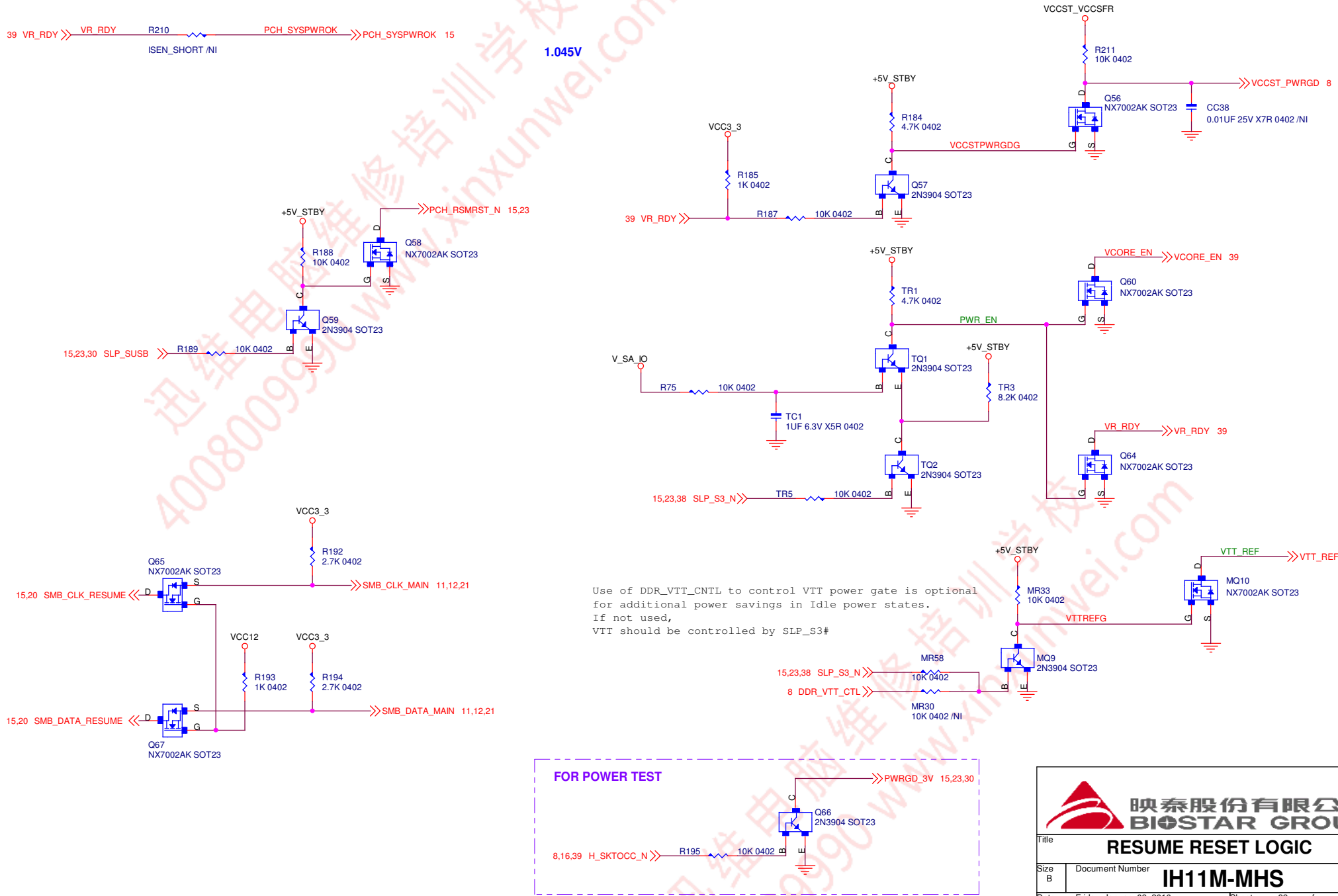
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Size	Document Number	IH11M-MHS	
B		Rev 6.0	
Date:	Friday, January 08, 2016	Sheet	32 of 42



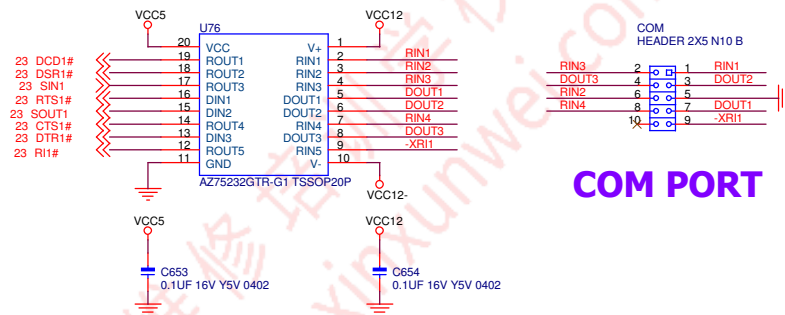




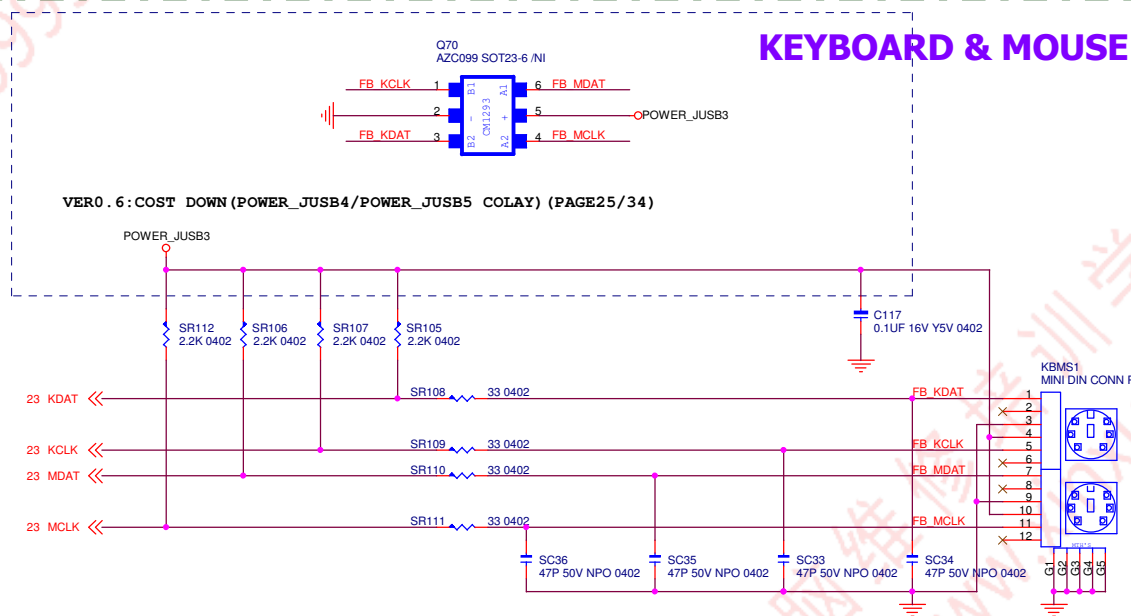
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Size	Document Number		IH11M-MHS		Rev
B					6.0
Date:	Friday, January 08, 2016		Sheet	33	of 42



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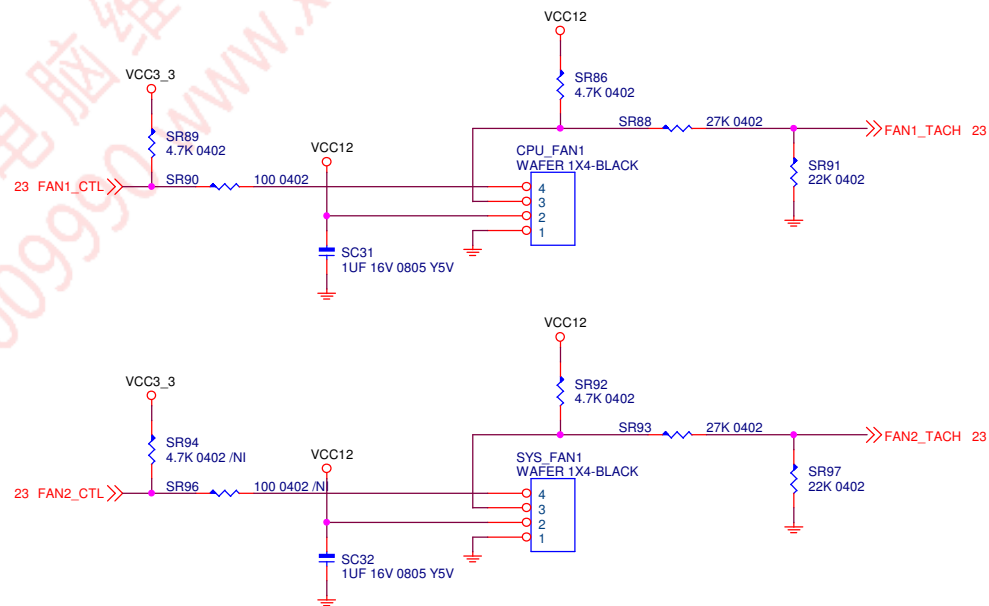
COM1 / PS2 CONN

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Document Number  
**IH11M-MHS**

Rev  
6.0

Sheet 34 of 42



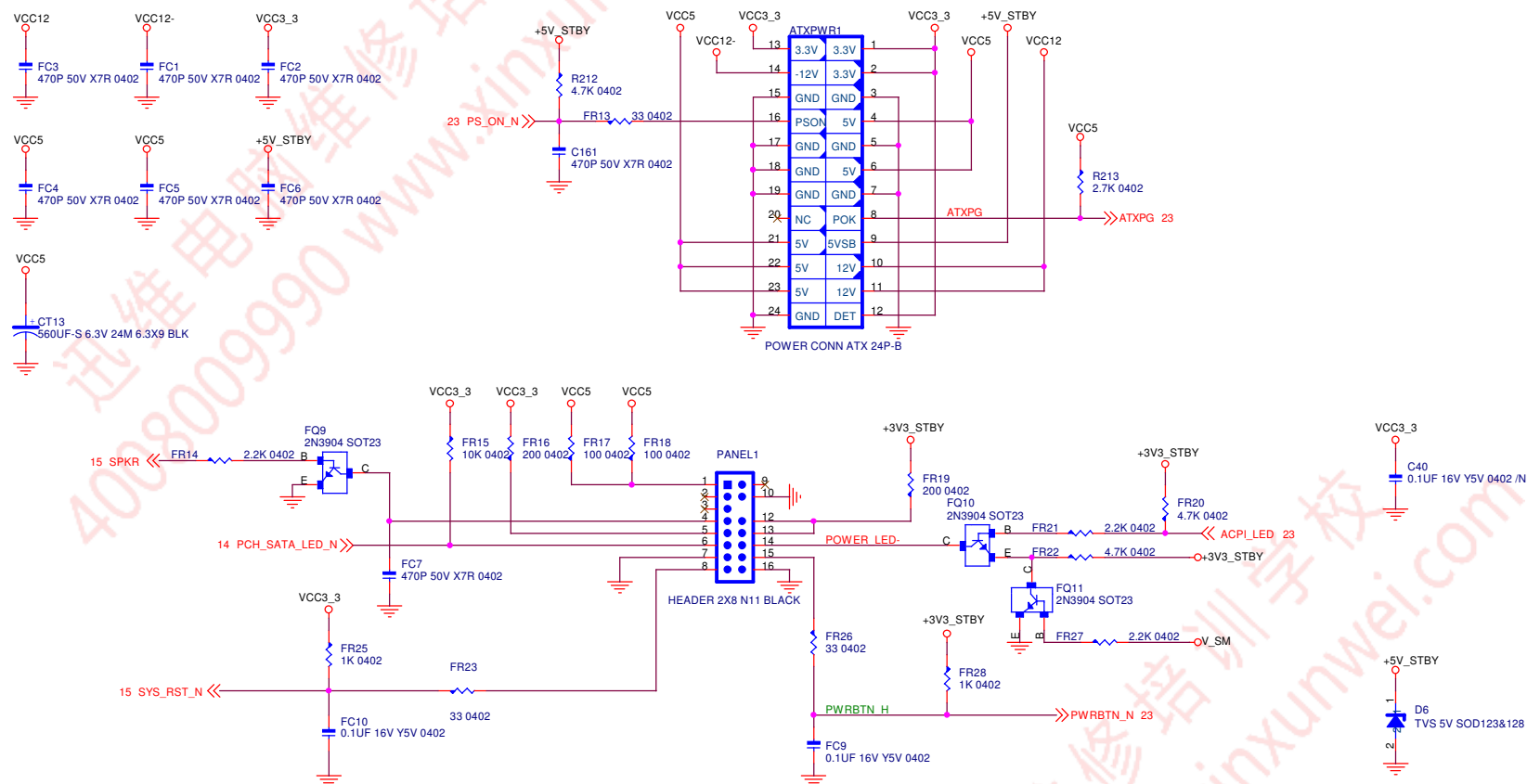
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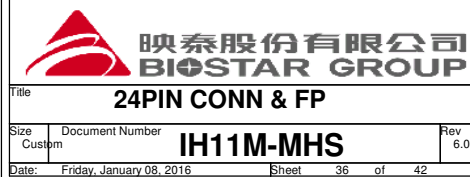
Title			FAN & PS2
Size	Document Number	IH11M-MHS	
B		Rev	6.0
Date: Friday, January 08, 2016		Sheet	35 of 42

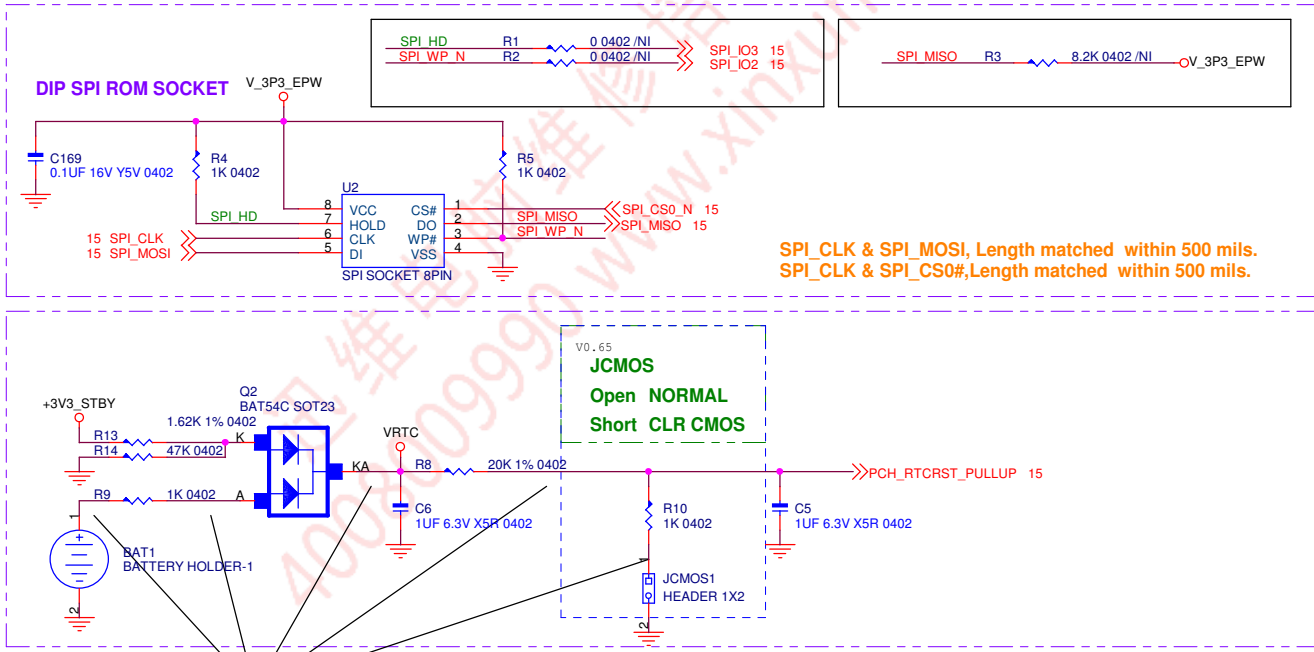
## FP PART: F+Reference



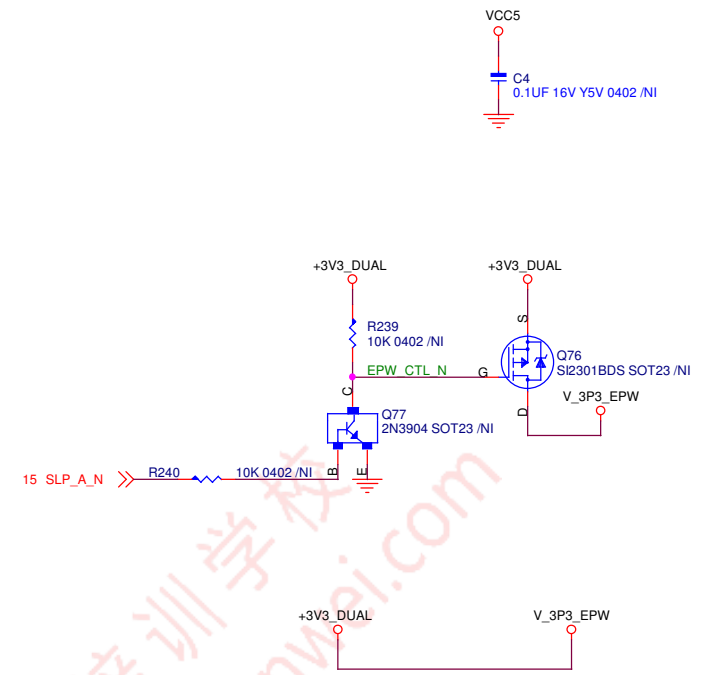
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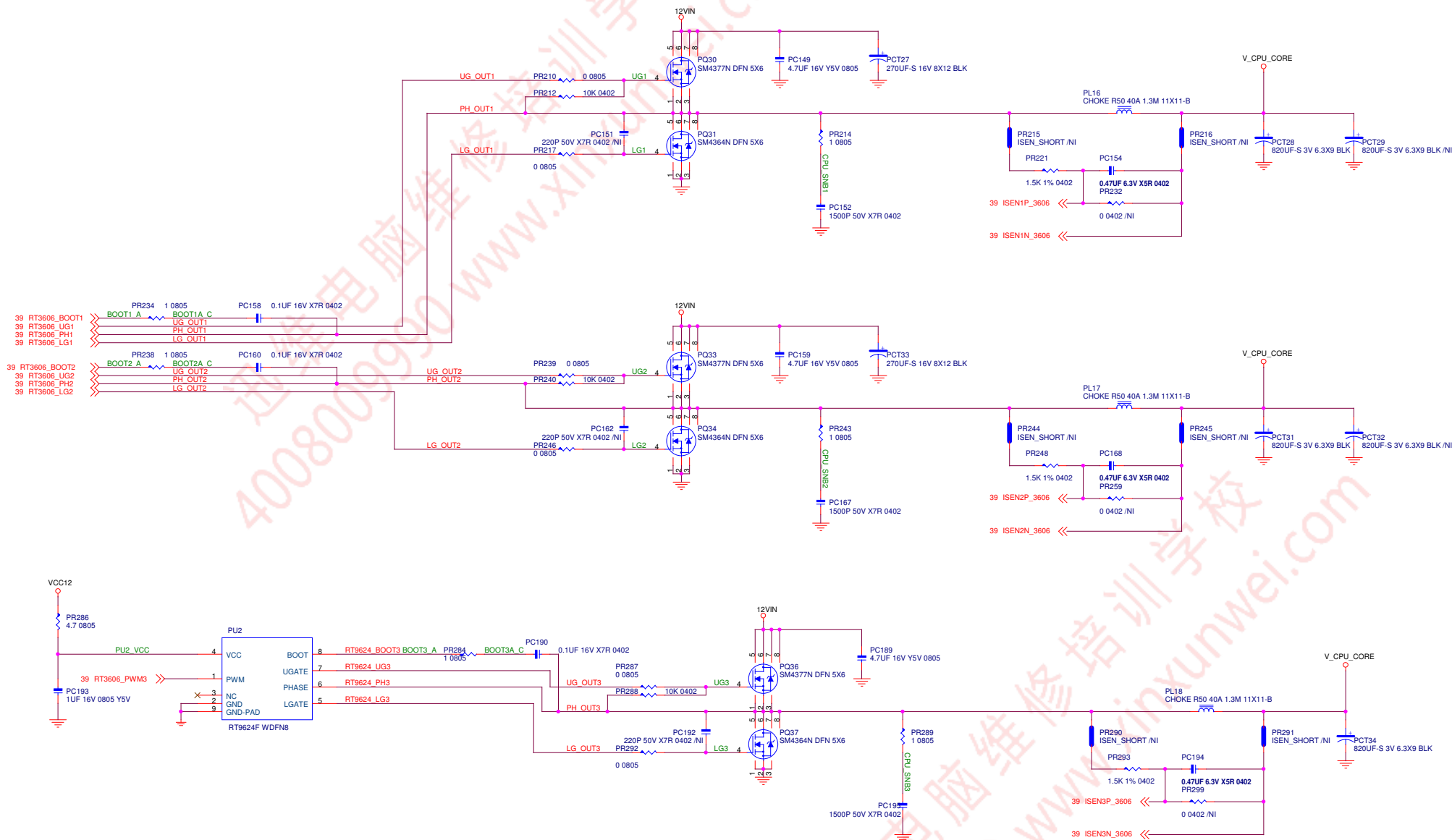
Title **SPI ROM/RTC CRYSTAL/BAT**

Size B	Document Number <b>IH11M-MHS</b>	Rev 6.0
Date: Friday, January 08, 2016		Sheet 37 of 42

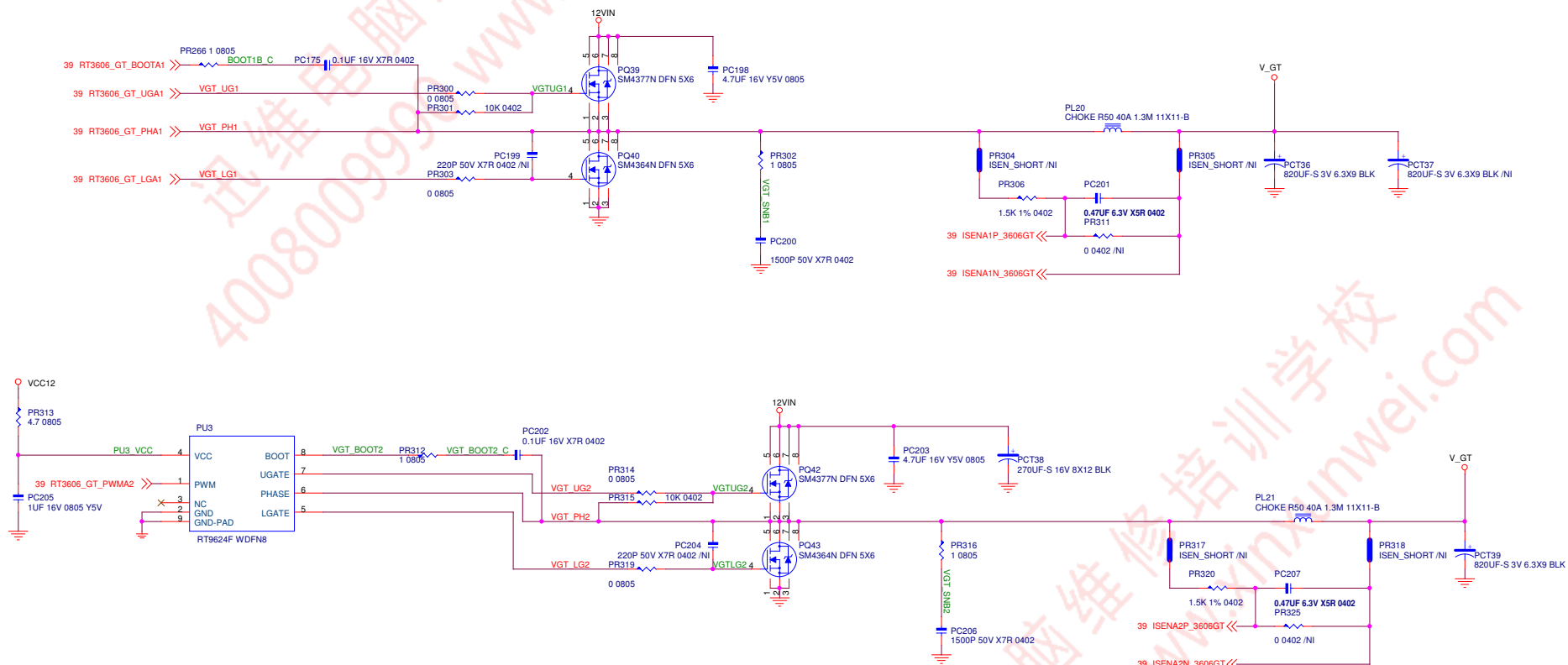


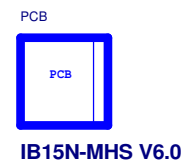
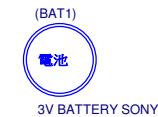
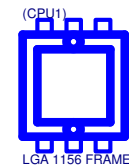
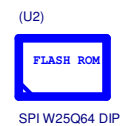
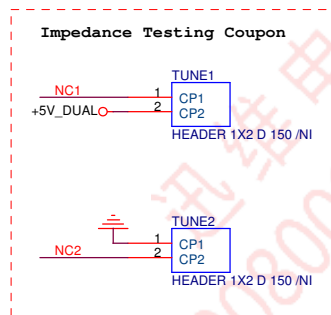
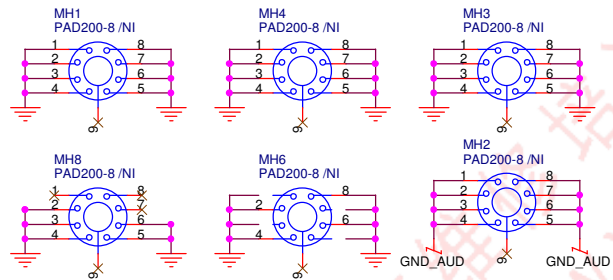






# Skylake S-line 42 95W RT3606\_VGT





Title			BOM
Size	Document Number	IH11M-MHS	
B			Rev 6.0
Date:	Friday, January 08, 2016	Sheet	42 of 42